Wandel & Goltermann
Elektronische Meßtechnik

PJM-4
Jitter Meter

BN 2019, series A onwards

Service Manual

Wandel & Goltermann
Electronic Measurement Technology

Please direct all enquiries to your local Wandel & Goltermann sales company. The adresses are given at the end of this handbook.

Wandel & Goltermann GmbH & Co
Electronic Measurement Technology
Product Documentation Department
Mühleweg 5, D-7412 Eningen u. A.
© 1991

Text: R. Huberty
Layout:
P. Ratmachers, U. Schenk

Order no.: BN 2019/00.83
Edition: 50/91.05, A onwards

Previous editions:
3974/90.07, A onwards

Printed in Germany

Service concept 1

Important notes 2

Mechanical design, maintenance 3

Troubleshooting: Localization to faulty assembly 4

Troubleshooting: Localization to faulty circuit board 5

Troubleshooting: Localization to faulty component 6

Alignment instructions 7

Verification of technical data 8

Functional and circuitry description 9

Tables, diagrams 10

1 SERVICE CONCEPT 1-1

1.1 Introduction 1-1
1.2 Measuring equipment 1-6
1.3 Tools 1-7

2 IMPORTANT NOTES 2-1

2.1 Safety measures 2-1
2.2 Circuit protection 2-2
2.3 Measuring technique, repair aids 2-3
2.4 Soldering instructions 2-14

3 MECHANICAL DESIGN, MAINTENANCE 3-1

3.1 Instrument data 3-1
3.2 Location of assemblies 3-2
3.3 Assembly instructions 3-7
3.4 Installing options 3-14
3.5 Maintenance work 3-15
3.6 Cleaning work 3-15

4 TROUBLESHOOTING: LOCALIZATION TO FAULTY ASSEMBLY 4-1

4.1 General notes on troubleshooting 4-1
4.2 Self-test for fault localization 4-1
4.3 Service programs 4-5
4.4 Monitor programs (woris functions) 4-6
4.5 Troubleshooting in the measuring section 4-7
4.6 Possibilities for swapping circuits and/or functional groups 4-28
4.7 Special test setups 4-31
4.8 Circuit-related block circuit diagram 4-41
4.9 Booting 4-41

5 TROUBLESHOOTING IN FUNCTIONAL GROUPS 5-1

5.1 Frequency generator (A) 5-1
5.2 Input circuit [2/2019-V] (B) 5-4
5.3 Code error 1 and 2 [3/2019-AL], [4/2019-AO] (C) 5-10
5.4 220 MHz circuit (D) 5-14
5.5 11 MHz circuit (E) 5-20
5.6 Adder [10/2019-AF] (F) 5-28
5.7 RF control [14/2019-AF] (G) 5-34
5.8 Filter/Rectifier [11/2019-Y/Z] (H/K) 5-37
5.9 Hit counter [13/2019-AA] (I) 5-46
5.10 Display/control section (L) 5-48
5.11 Power supply unit (N) 5-58

6 TROUBLESHOOTING: LOCALIZATION TO FAULTY COMPONENT 6-1

6.1 General notes on troubleshooting and repairs 6-1
6.2 Troubleshooting in the carrier oscillator [5/2019-P] 6-1
6.3 Troubleshooting in the carrier phase meter [6/2019-Q] 6-1
6.4 Troubleshooting in lock-in oscillator [6/2019-R] 6-2
6.5 Troubleshooting in the 220 MHz VCO [7/2019-M] 6-2
6.6 Functional check of controller 2 [7/2019-N] 6-3
6.7 Sawtooth phase meter [7/2019-O] 6-5
6.8 Mixer [7/2019-U] 6-12
6.9 11 MHz phase meter [8/2019-G] 6-13
6.10 Troubleshooting in the 11 MHz VCO [8/2019-J] 6-13
6.11 Functional check, controller 1 [9/2019-J] 6-14
6.12 Troubleshooting the CPU-2, BN 965, circuit diagram (90) 6-16
6.13 Troubleshooting the IEEE 488 /<IEC 625> Interface bus card BN 958, circuit diagram (91) 6-25
6.14 Troubleshooting in the power supply unit 6-26

7 ALIGNMENT INSTRUCTIONS 7-1

7.1 Alignment summaries 7-1

8 VERIFICATION OF TECHNICAL DATA 8-1

8.1 Introduction 8-1
8.2 Function tests 8-2
8.3 Return losses 8-6
8.4 Input sensitivity, equalization 8-8
8.5 Synchronization, counting mode 8-12
8.6 Jitter measuring accuracy 8-14

9 FUNCTIONAL AND CIRCUITRY DESCRIPTION 9-1

9.1 Functional description 9-1
9.2 Circuitry description 9-19
9.3 Software description 9-100

10 BLOCK CIRCUIT DIAGRAMS 10-1

FIGURES

1.1-1 Repair sequence for a faulty instrument ... 1-2
1.1-2 Test strategy for instruments with microprocessor controller ... 1-3
1.2-1 Measuring instruments ... 1-6
1.2-2 List of auxiliary equipment ... 1-7
1.3-1 List of tools ... 1-7

2.3-1 Component families ... 2-3
2.3-2 Basic ECL circuit ... 2-3
2.3-3 Transfer characteristic ... 2-4
2.3-4 Wired OR combinatorial circuit ... 2-4
2.3-5 Earthing plate (102-911) ... 2-4
2.3-6 Earthing plate (101-911) ... 2-5
2.3-7 Earthing spring (103-911) ... 2-5
2.3-8 Earthing spring (104-911) ... 2-5
2.3-9 Probe adapter ... 2-5
2.3-10 Making measurements on SMDs ... 2-6
2.3-11 Elementary circuit diagram of a signature analyzer ... 2-7
2.3-12 DIL switch S1 on the adapter board, basic settings ... 2-11
2.3-13 Adapting the MONEX 1130 to the PJM-4 ... 2-12
2.4-1 Outline drawings of SMDs ... 2-15
2.4-2 Desoldering a SMD ... 2-16
2.4-3 Illustrations of good and bad solder joints ... 2-17

3.1-1 Instrument data ... 3-1
3.2-1 Top view of PJM-4 ... 3-2
3.2-2 PJM-4 from below, with power supply unit and storage batteries of Series B ... 3-3
3.2-3 "RF block" swung up ... 3-4
3.2-4 "RF block" swung out ... 3-5
3.2-5 Power supply unit, Series A ... 3-6
3.3-1 Dismantling the instrument ... 3-7
3.3-2 Shielding troughs and frames ... 3-8
3.3-3 Replacing key caps or spring inserts ... 3-10
3.3-4 Top view after removing the front panel ... 3-12

4.5-1 Table: Measured values for basic noise ... 4-18
4.5-2 Basic noise, mid-band with reference line ... 4-20
4.5-3 Noise magnitude, frequency generator ... 4-20
4.5-4 Hum lines ... 4-21
4.5-5 Fault localization table - part 1 ... 4-22
4.5-5 Fault localization table - part 2 ... 4-23
4.5-6 Table of circuits causing inherent noise ... 4-23
4.6-1 Table: effects of swapping individual circuits ... 4-29
4.7.2-1 Test setup for testing the inherent jitter for clock signals ... 4-35
4.7.2-2 Test setup for testing the inherent jitter for data signals ... 4-37
4.7.3-1 Test setup for testing the control limit frequency of the 220 MHz circuit ... 4-39

5.2-1 Input circuit level diagram ... 5-9
5.5.2-1 Test setup for measuring the frequence response of the 11 MHz circuit ... 5-24
5.5.2-2 Typical frequency response of the 11 MHz circuit ... 5-25
5.6.2-1 Table ... 5-31
5.11-1 Comb plug [2019-AS] as test device ... 5-59
5.11-2 Troubleshooting diagram, power supply unit ... 5-60

6.11-1 Fast/slow switching operation ... 6-15
6.12-1 Settings of the service and free-run switch S1 ... 6-16
6.12-2 DIL switch setting ... 6-17
6.12-3 ROM test procedure - addition of memory contents ... 6-18
6.12-4 I/O module activation ... 6-19
6.12-5 Value of the data bits for free-running ... 6-20
6.12-6 Structural diagram of troubleshooting ... 6-21
6.12-7 Edge assignment of the START/STOP frame ... 6-22
6.12-8 Address signatures (CPU board) ... 6-23
6.12-9 RAM signatures (data lines) ... 6-24
6.13-1 DIL switch settings for IEC bus test ... 6-25
6.14-1 Functional check of the DC/DC converters ... 6-29
6.14-2 Terminal assignments with plug-in card [2019-AU] ... 6-29
6.14-3 Terminal assignments without plug-in card [2019-AU] ... 6-30
6.14-4 Synchronization signal ... 6-31

7.1.1-1 Alignment elements ... 7-1
7.1.1-1 Alignment elements (contd.) ... 7-2
7.1.1-1 Alignment elements (contd.) ... 7-3
7.1.2-1 Alignment work after replacement/alignment of boards ... 7-4
7.1.2-1 Alignment work after replacement/alignment of boards (contd.) ... 7-5
7.1.3-1 Alignment work after replacement of assemblies ... 7-6

7.2.1-1 Sideband noise alignment ... 7-7
7.2.1-2 Alignment for minimizing the inherent jitter display ... 7-8
7.2.1-3 Approximate values for total resistance and trimmer P ... 7-9
7.2.2-1 Test setup for alignment of the input circuit frequency response ... 7-10
7.2.2-2 Test setup for signal amplitude alignment ... 7-11
7.2.2-3 Test setup for threshold alignment 2 P 3 ... 2 P 5 ... 7-12
7.2.3-1 Test setup for code error card 1 alignment ... 7-13
7.2.3-2 Signal diagram (20) ... 7-15
7.2.4-1 90° phase alignment ... 7-21
7.2.5-1 Incorrect alignment of P 1 ... 7-24
7.2.5-2 Incorrect alignment of P 1 ... 7-24
7.2.5-3 Correct alignment of P 1 ... 7-24
7.2.6-1 Delay settings ... 7-26
7.2.6-2 Test setup for adder alignment ... 7-26
7.2.6-3 Typical frequency responses, 220 MHz circuit; control limit frequency 2 kHz ... 7-30

8.2-1 Test setup for jitter measurements ... 8-2
8.2-2 Table for input signal settings ... 8-2
8.2-3 Test setup for phase hit measurements ... 8-3
8.2-4 Table for phase hit measurements ... 8-4
8.2-5 Test setup for detecting code errors ... 8-5
8.2-6 Table for code error detection ... 8-5
8.3-1 Test setup for return loss measurements in the range 10 kHz ... 15 MHz ... 8-6
8.3-2 Table for return loss measurements in the range 10 kHz ... 15 MHz ... 8-6
8.3-3 Test setup for return loss measurements in the range 15 MHz ... 180 MHz ... 8-7
8.3-4 Test setup for return loss measurements up to 210 MHz ... 8-8
8.4-1 Test setup for measuring the input sensitivity ... 8-9
8.4-2 Test setup for testing the external clock input ... 8-10
8.4-3 Test setup for testing the equalizer ... 8-10
8.5-1 Test setup for testing synchronization ... 8-12
8.5-2 Table for testing synchronization ... 8-13
8.5-3 Test setup for counting mode ... 8-13
8.6-1 Test setup for measuring the basic noise ... 8-15
8.6-2 Basic noise with clock signal ... 8-15
8.6-3 Basic noise with data signal ... 8-16
8.6-4 Test setup for jitter display ... 8-16
8.6-5 Table for the linearity test ... 8-18
8.6-6 Table for testing the frequency response ... 8-20

9.1-1 Simplified representation of the jitter meter function ... 9-3
9.1-2 Simplified block circuit diagram, part 1 ... 9-6
9.1-2 Simplified block circuit diagram, part 2 ... 9-7
9.1-3 Lock-in aid, 220 MHz circuit ... 9-12
9.1-4 11 MHz lock-in aid ... 9-13
9.1-5 Instrument in "normal" mode ... 9-14
9.1-6 Status diagram for the synchronization sequence ... 9-16
9.1-7 Status diagrams for program modules ... 9-17
9.1-8 Setting table for control circuits ... 9-18
9.2-1 "Internal" setting ... 9-20
9.2-2 "External" setting ... 9-21
9.2-3 "Internal" <-> "External" switching ... 9-21
9.2-4 Code error 1 ... 9-26
9.2-5 Sampling circuit ... 9-28
9.2-6 CMI coding and sampling ... 9-28
9.2-7 CMI code error detector ... 9-29
9.2-8 Timing diagram of the data sampler and error detector for CMI ... 9-30
9.2-9 AMI/HDB-3 coding and sampling ... 9-31
9.2-10 HDB-3 coding ... 9-32
9.2-11 Selectable error criteria ... 9-33
9.2-12 AMI/HDB-3 detector ... 9-33
9.2-13 Timing diagram of the data sampler and error detector for AMI ... 9-34
9.2-14 Timing diagram of the data sampler and error detector for HDB-3 ... 9-35
9.2-15 Timing diagram of the HDB-3 zero detector ... 9-36
9.2-16 Input sensitivity as a function of switch setting ... 9-37
9.2-17 Multiplexer truth table ... 9-37
9.2-18 Block circuit diagram, code error 2 ... 9-39
9.2-19 Code table, MMS 43 (BP) code ... 9-40
9.2-20 Non-scrambled continuous "1" sequence in 4B3T code (MMS 43) ... 9-41
9.2-21 Example of B3T coding and error evaluation ... 9-41
9.2-22 5B6B code table ... 9-42
9.2-23 RDS and error pulse formation ... 9-43
9.2-24 4B3T code error evaluation ... 9-44
9.2-25 Operating table ... 9-44
9.2-26 5B6B code error evaluation ... 9-45
9.2-27 Operating table ... 9-45
9.2-28 Simplified block circuit diagram, controller 2 ... 9-47
9.2-29 Functional principle ... 9-49
9.2-30 Phase measuring range ... 9-53

9.2-31 Misalignment, controller 1 ... 9-55
9.2-32 Misalignment, controller 1 ... 9-55
9.2-33 Overall lock-in process, 11 MHz loop. Controller 1 correctly aligned ... 9-56
9.2-34 Block circuit diagram ... 9-58
9.2-35 Block circuit diagram, filter (11) ... 9-61
9.2-36 Gain setting on the peak rectifier ... 9-65
9.2-37 Block circuit diagram, peak rectifier ... 9-66
9.2-38 Amplifier [2019-7031] ... 9-67
9.2-39 Negative peak value meter ... 9-68
9.2-40 Timing diagram of pulse generation ... 9-70
9.2-41 Data polling on the A/D converter ... 9-71
9.2-42 Divider control ... 9-71
9.2-43 Block circuit diagram, PJM-4 power supply unit ... 9-82
9.2-44 Block circuit diagram of the DC/DC converter ... 9-84
9.2-45 Connecting terminals of the converter ... 9-84
9.2-46 Block circuit diagram ... 9-85
9.2-47 Reset function following a data-save signal ... 9-87
9.2-48 Connection of U_{Bat} to 5 V supply ... 9-89
9.2-49 Value of the data bits for free-running ... 9-91
9.2-50 Generation of the LSS signal ... 9-92
9.2-51 IO timing ... 9-93
9.2-52 Signal sequence for counter overflow ... 9-93
9.2-53 Timing control sequence - general situation ... 9-94
9.2-54 Test points ... 9-95
9.2-55 Block circuit diagram of the IEEE 488/<IEC 625> interface bus card ... 9-96
9.2-56 Structure of the IEC bus program ... 9-99
9.3-1 Key assignments in "SERVICE" mode ... 9-106

1 SERVICE CONCEPT 1-1

1.1 Introduction 1-1
1.1.1 Troubleshooting strategy 1-3
1.1.1.1 Fault localization strategy for assembly or circuit board (Section 4 or 5) 1-3
1.1.1.2 Fault localization strategy for components (Section 6) 1-4
1.1.2 Ordering spare parts 1-4
1.1.2.1 General 1-4
1.1.2.2 Replacing the "RF block" 1-5
1.1.2.3 Replacing the DC/DC converter 1-5

1.2 Measuring equipment 1-6
1.2.1 Measuring instruments 1-6
1.2.2 Auxiliary equipment 1-7

1.3 Tools 1-7

1 SERVICE CONCEPT

1.1 INTRODUCTION

Maintenance, repairs and calibration are the main tasks involved in servicing a measuring instrument.
All the necessary information is provided in the Description and Operating Manual, together with the Service Manual and the Appendix.

The Description and Operating Manual provides all the necessary information on the instrument, such as technical data, commissioning and notes on measurements. Simple non-electrical maintenance work is also described.

The Service Manual and the Appendix provide all the specific information required for repairs and calibration.
The time taken for fault localization and repair should be as short as possible. Together with the Appendix, the Service Manual offers all the necessary assistance in this context.

Various service tools allow rapid detection of faulty functional assemblies.
Emphasis should be placed on the comprehensive test programs and the monitor program. Depending on the type of fault and the measuring equipment and tools available, this service tools can enable repairs to be made down to the component level.

A simplified repair sequence and the subdivision of troubleshooting into three stages (levels) is shown in Fig. 1.1-1.

In addition to repairs, calibration is also necessary at certain intervals, i.e. verification of the technical data. Section 8 of these Service Manuals describe this work in detail.

Test programs are available for efficient functional testing. Please address all enquiries to Customer Service (Department VBS).

The Appendix to the Service Manual contains all the general block diagrams, circuit diagrams and component layout diagrams of the assemblies and circuit boards, together with the corresponding parts lists for ordering spare parts.

Corresponding Section in Service Manual	
No.	Designation
4	Localization to faulty assembly (Top level)
5	Troubleshooting, localization to faulty circuit board (Middle level)
6	Troubleshooting, localization to faulty component (Bottom level)
2	Important notes
7	Alignment instructions
8	Verification of technical data

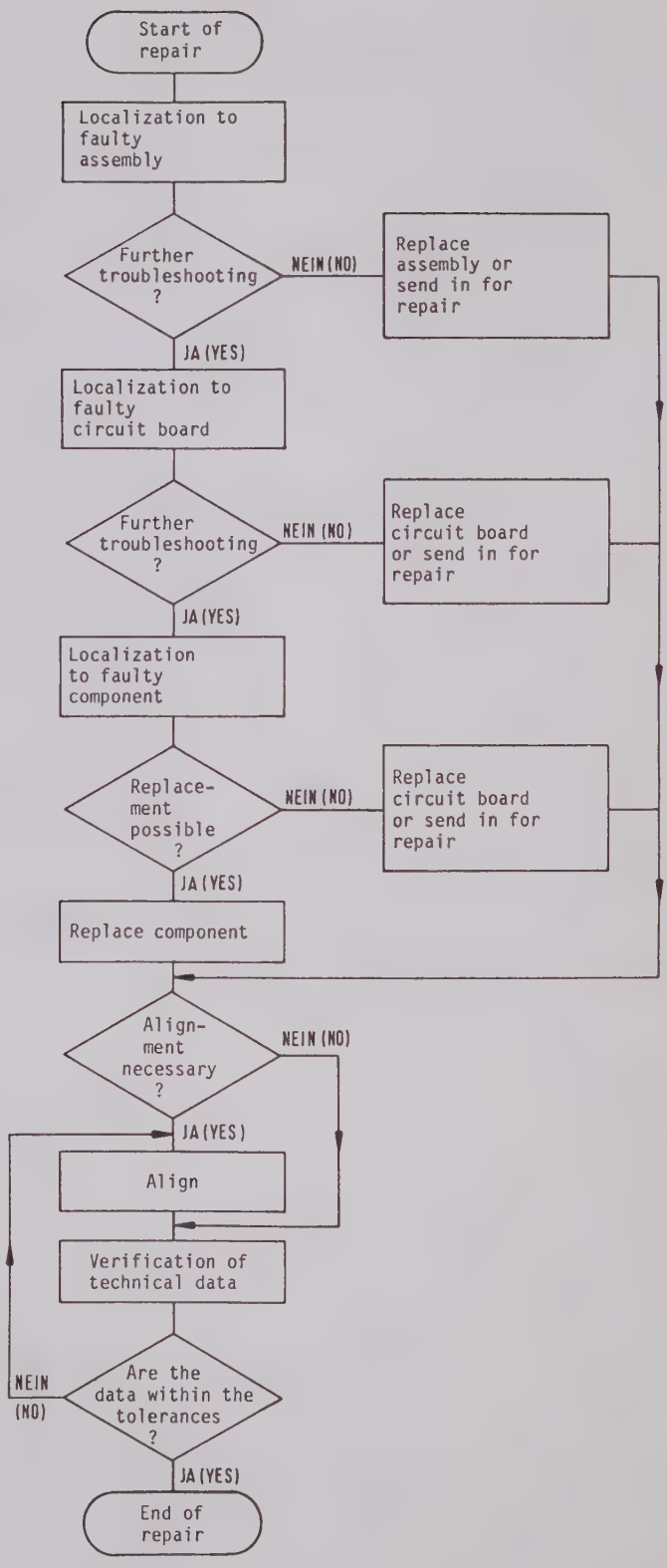


Figure 1.1-1 Repair sequence for a faulty instrument

1.1.1 TROUBLESHOOTING STRATEGY

The right test strategy always starts at the heart, the microprocessor, and works outwards. Refer to Fig. 1.1-2.

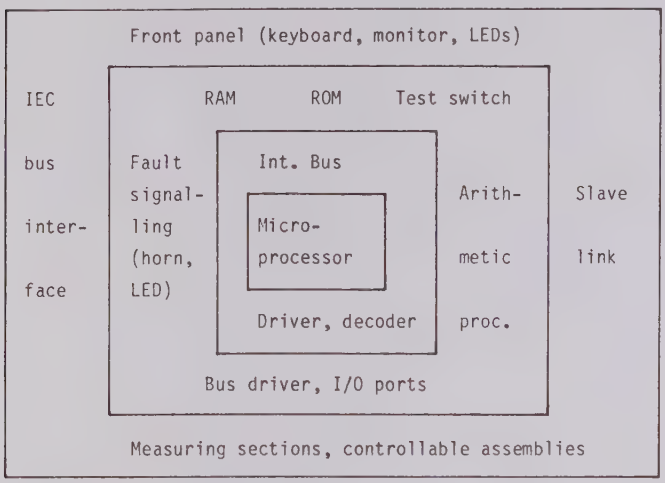


Fig. 1.1-2 Test strategy for instruments with microprocessor controller

The Sections on troubleshooting are arranged in the same form as the instrument. This facilitates fault localization.
The following two Sections describe the fault localization strategy, also showing the differences in the measuring equipment required for different objectives - repair down to the component level or only circuit board replacement.

1.1.1.1 Fault localization strategy for assembly or circuit board

(Section 4 or Section 5)

Fault localization tools:
- Measuring equipment: Only simple instruments or auxiliary equipment are required, if any!
- Software tools:

a) Switching on starts the so-called "Confidence Check". This self-test in the processor section checks the memories, bus systems with drivers and decoders and the arithmetic processor, as well as the most important instrument functions.

b) Built-in service programs. These programs must be called up separately, either via the front panel keybord or via DIL switches on a CPU board.
Unlike the Confidence Check, these tests are far more stringent. In some cases, even faulty components can be identified.

c) The monitor program. This program is operated either via the front panel or via the external "MONEX" control unit. Gates and memories can be read and written, as well as starting programs.

Wherever possible, error numbers or similar displays indicate a certain functional group in the instrument.

1.1.1.2 Fault localization strategy for components (Section 6)

Fault localization tools:

- Measuring equipment: Depending on the type of fault, the measuring equipment listed (Section 1.2) should be available.
- Software tools:

a) Hardware-oriented repair programs, cyclic and non-repeating.
   These programs are called up, for example, via the front panel or via DIL switches.
   The "Confidence Check" may also indicate a faulty component.

b) Free running of the microprocessor for signature analysis. Troubleshooting in the heart of the microcomputer circuitry (EPROMs, decoder ...).

c) Stimulus programs for troubleshooting with signature analysis.
   These programs are required in the I/O area, for example.

d) The monitor program. This can also be a great help in troubleshooting at the component level.

The Circuitry Description in Section 9 of these Service Manuals is also of major assistance.

1.1.2 ORDERING SPARE PARTS

1.1.2.1 General

Please note the following when ordering spare parts:

- The precise designation can be found in the electric parts list (in the Appendix).
- Components with BV or WN must be requested from the manufacturer.

In addition to the Order No. (BN), the following data must be quoted:

- Instrument type and instrument number with Series index
- Card index or Item No. of the component
- Subject No.

Examples:

Circuit board
PCM-4 BN 984/01
No. A-0062
Card: 984-E

Component
PCM-4 BN 984/01
No. A-0062
Component: 2 T 2

Circuit diagram number — Item number

Subject No.: 0001-0015.836

1.1.2.2 Replacing the "RF block"

The RF block contains the crystals for the bit rates of the PJM-4. The bit rates comprise the basic bit rate (basic version) and the customer-specific bit rates (option).
Specially-manufactured crystals are used for each customer-specific bit rate (option).
In view of the great number of different option crystals, it is impossible to keep a stock purely for repair purposes. Therefore, if servicing (replacement) is required, only an "RF block" with the crystals of the basic version can be provided.
The option crystals must be transferred from the faulty "RF block" to the replacement "RF block" on the user's premises. Do not return the faulty "RF block" until the replacement "RF block" has been received and, if necessary, converted.

IMPORTANT:

When ordering, always state the basic version of the PJM-4.

The instrument data can be found on the rear of the PJM-4. They show the basic version of the instrument in question.

See Section 3.1 for further details.

1.1.2.3 Replacing the DC/DC converter

When replacing the DC/DC converter, make sure that the replacement converter is compatible with the one being replaced.

The production version of each DC/DC converter is indicated by a multi-digit number on the mounting bracket of the converter.
Always state this number with enquiries and orders.

1.2 MEASURING EQUIPMENT

1.2.1 MEASURING INSTRUMENTS

The measuring instruments listed here as necessary for testing represent a recommendation only. Equivalent instruments from other manufacturers may also be used.

Instrument	Requirements	Rec. Type Order No.	Manufacturer	In Section 4/5	6	7	8
Spectrum and network analyzer	10 kHz ... 180 MHz	SNA-1 Type 02 BN 956	W&G	x		x	x
Spectrum analyzer	... 400 MHz	TEK 495 A	TEK	x		x	
1x active test probe	... 400 MHz	TEK P 6201	TEK	x		x	
1x test probe 500 Ω	... 400 MHz	TEK P 6056	TEK			x	
Oscilloscope	Bandwidth $\geq$ 350 MHz Z = 50 Ω	TEK 2465	TEK	x	x	x	x
Level generator	100 Hz ... 25 MHz	PS-19	W&G	x		x	x
Selective level meter	100 Hz ... 25 MHz	SPM-19	W&G	x		x	x
Active test probe	... 180 MHz	TK-11	W&G	x		x	x
Sine-wave generator	... 160 MHz	PSS-16	W&G	x	x	x	
Jitter generator	2, 8, 34, 139 Mbit/s Mod.: up to 16 UI_{pp}, up to 5 MHz	PJG-4	W&G	x	x	x	x
Bit error measuring set	2, 8, 34, 139 Mbit/s Code error	PF-4	W&G				x
Digital multimeter	4 1/2-digit	8050 A, 8600 A	Fluke			x	
Transient recorder	Sampling rate ... 2 MHz	TR-940	W&G			x	
Return loss measuring attachment	10 kHz ... 15 MHz	RFZ-5	W&G				x
Reflection coefficient meas. bridge	15 MHz ... 180 MHz (210)	RFZ-4	W&G				x
Attenuator set	$f_o \geq$ 200 MHz Z = 75 Ω	D 2053	Siemens				x
RMS digital voltmeter	4 1/2-digit AC/DC	3478 A	HP	x	x	x	
Universal counter	... 400 MHz	PM 6672/421	Philips	x			

Fig. 1.2-1 Measuring instruments

1.2.2 AUXILIARY EQUIPMENT

Designation	Rec. Type Order No.	Manufacturer	In Section 4/5	6	7	8
BNC T-adapter ... 180 MHz	S 413	W&G	x		x	x
T-adapter ... 300 MHz	2 x 75 Ω BN 595/01	W&G	x	x	x	x
Adapter card	AK-3 (901/00.11) 901-7007.000	W&G			x	
RF cable 50 Ω	K 76	-				x
100 + 24 metre coax. cable	RG 59B/4	-			x	
Matching pad 50 Ω/75 Ω	ZA 5075/BN 925	W&G	x			
Attenuator 10 dB	DG-1410 BN 920/10	W&G	x			

Fig. 1.2-2 List of auxiliary equipment

1.3 T O O L S

Designation	Rec. Type Order No.	Manufacturer
Soldering station	WECP/20	Weller
Soldering tip	ET-B	Weller
Flat form	2.4 mm	
Flat form	ET-C 3.2 mm	Weller
Flat form (only in exceptional cases)	ET-L 2.0 mm	Weller
Flat form	ET-E 6.0 mm	Weller

Fig. 1.3-1 List of tools

2 IMPORTANT NOTES 2-1

2.1 Safety measures 2-1
2.1.1 Electrical safety 2-1

2.2 Circuit protection 2-2
2.2.1 Protection of MOS components 2-2

2.3 Measuring technique, repair aids 2-3
2.3.1 Component-specific measuring technique 2-3
2.3.1.1 Measuring technique for ECL ICs 2-3
2.3.1.2 Making measurements on SMD PCBs 2-6
2.3.2 Signature analysis 2-6
2.3.3 Monitor functions 2-8
2.3.3.1 Description of the basic functions of the monitor software 2-8
2.3.3.2 Basic configuration of the external control section MONEX 2-10
2.3.3.3 Service EPROM 2-11
2.3.4 Adaption and notes on using the external MONEX with the PJM-4 2-12

2.4 Soldering instructions 2-14
2.4.1 Soldering on curcuit boards of plated-through design 2-14
2.4.2 SMD PCB soldering and repair instructions 2-14
2.4.2.1 Introduction 2-14
2.4.2.2 Instructions for handling SMDs 2-15
2.4.2.3 SMD soldering and repair instructions 2-15

2 IMPORTANT NOTES

2.1 SAFETY MEASURES

2.1.1 ELECTRICAL SAFETY

Protection class

This instrument is classified in protection class I to VDE 0411 and IEC Publ. 348. The power cord supplied contains a non-fused earthed conductor. The mains plug may only be plugged into earthed sockets, except in specially approved rooms. The non-fused earthed conductor must not be interrupted either inside or outside the instrument.

Opening the instrument

Live parts may be exposed when covers are opened or parts removed with the aid of a tool. Connecting points may also be live.

The instrument must be disconnected from all power sources before being opened.

If it is essential to perform calibration, maintenance or repair work on the instrument when it is both open and connected to the power supply, such work must only be carried out by a specially trained mechanic who is aware of the potential danger.

Capacitors inside the instrument may still be charged, even if the instrument itself has been disconnected from all power sources; the circuit diagrams must be consulted.

Fuses

Only the specified fuses may be used.

Repairs, replacing parts

Repairs must be performed correctly. Particular care must be taken to ensure that the design features of the instrument are not altered in a manner reducing its safety. On no account must the creepage and air paths or the insulation distances be reduced.

Only use original parts as replacements. Other spare parts may only be used if they do not impair the safety characteristics of the instrument.

Testing after repair and maintenance work

Testing the non-fused earthed conductor

Visually check for correct connection and good condition of the conductor and measure the resistance between the plug connection of the non-fused earthed conductor and the housing. The resistance should be <0.5 Ω. Move the connecting lead during this measurement. Fluctuations in the resistance are indicative of damage to the conductor.

Testing the insulation resistance

Measure the insulation resistance between the mains connections and the non-fused earthed conductor at a voltage of 500 V DC. Set the line switch on the instrument to "ON" for this purpose. The insulation resistance should be > 2 MΩ.

2.2 CIRCUIT PROTECTION

2.2.1 PROTECTION OF MOS COMPONENTS

Be careful when handling MOS components!

A number of MOS (metal-oxide semiconductor) components are used in this instrument. They can easily be damaged or destroyed by static charges, ripple voltages from unearthed devices or other interference voltages. Damage to the gate insulation does not always lead to immediate component failure, but often only after a certain period of operation. Damage due to static charges can be avoided by noting the following rules:

- Whenever possible, MOS components should remain in the supplier's wrapping until required. All connections must be conductively linked until used (black, electrically conductive foam).
- The electrically conductive part of the packaging must make contact with a reference potential in the form of a conductive worktop or the chassis of the instrument to be repaired before unpacking the MOS components or the circuit boards fitted with such components.
- Before touching the MOS components, touch the conductor acting as reference potential with one hand.
- All tools and instruments, the part to be repaired and the user should have the same potential as the conductor acting as the reference potential (e.g. a conductive worktop or, alternatively, the chassis of the instrument to be repaired). For this reason, first make contact between the reference potential and the tools with which the MOS components are to be handled. Tools must not have insulated handles.
- If work is being carried out on a circuit board or other instrument parts separately from the rest of the instrument and not on a conductive worktop, connect the earth of the circuit board, etc. to the reference potential.

Damage due to ripple voltages during soldering work can be avoided by establishing a permanent connection between the soldering iron and the chassis of the instrument being repaired.

MOS components can be recognized by the letters "MOS", as in CMOS, HCMOS or MOSFET, in the component designations of the electrical parts list.

2.3 MEASURING TECHNIQUE, REPAIR AIDS

2.3.1 COMPONENT-SPECIFIC MEASURING TECHNIQUE

2.3.1.1 Measuring technique for ECL ICs

The high clock frequency of the PF-4 requires the use of ECL components (refer to Fig. 2.3-1).

Designation	Gate delay, ns
TTL	10
LS-TTL	9
S-TTL	3
10 k ECL	2
ALS	3.5
FAST	2
100 k ECL	0.75

Fig. 2.3-1 Component families

Emitter-coupled logic (ECL) uses non-saturated switching transistors.

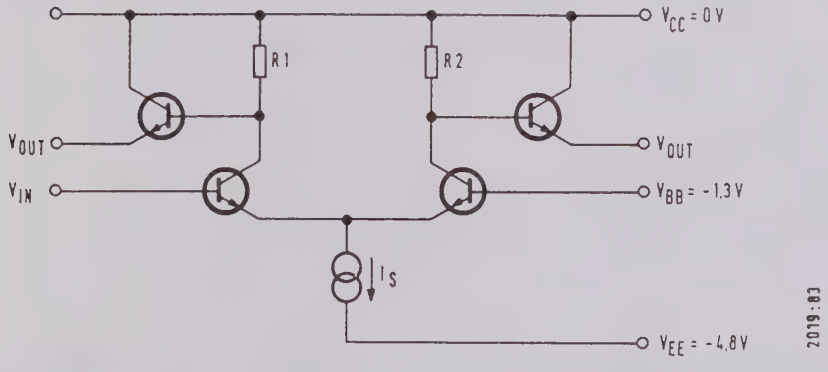


Fig. 2.3-2 Basic ECL circuit

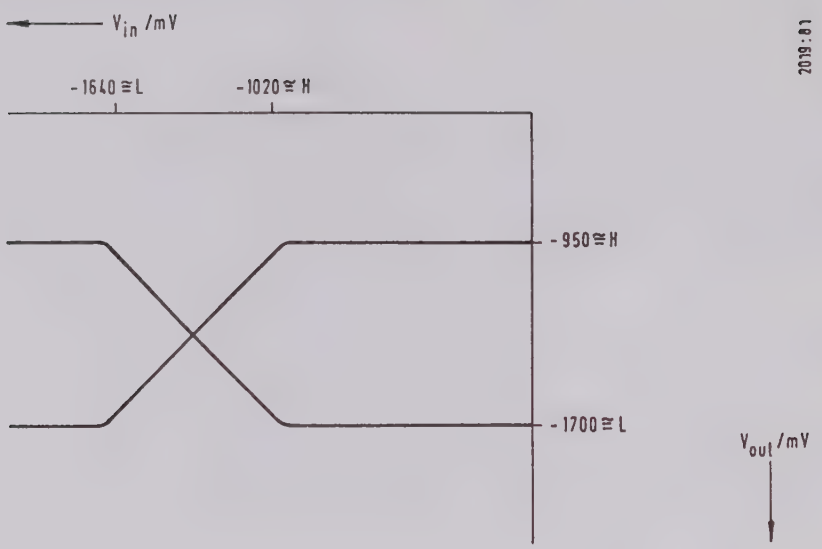


Fig. 2.3-3 Transfer characteristic

The ECL technique allows the formation of wired OR combinatorial circuits.

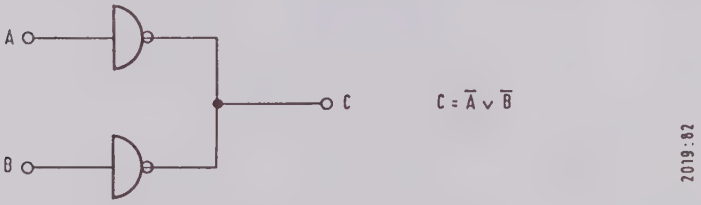
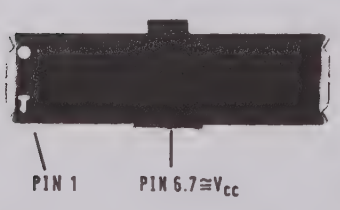


Fig. 2.3-4 Wired OR combinatorial circuit

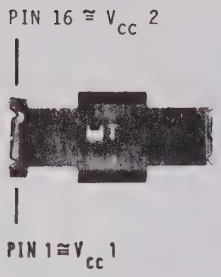
"500 Ω probes" (10:1 probe for connection to the 50 Ω input of an oscilloscope) are particularly suitable for testing ECL ICs with an oscilloscope. These probes ensure low-capacitance and low-return-loss coupling to terminated systems.

It is advisable to use special earthing plates and earthing springs in order to obtain "good" probe/earth connections.



For fitting on 100 k series ECL ICs

Fig. 2.3-5 Earthing plate (102-911)



For fitting on 10 k series ECL ICs[1)]

Fig. 2.3-6 Earthing plate (101-911)

For fitting on the probe

Fig. 2.3-7 Earthing spring (103-911)

For fitting on the probe

Fig. 2.3-8 Earthing spring (104-911)

For measurements on IC Pins, the associated earth connection can be tapped directly on the earthing plate, using the slip-on probe earthing spring (104-911). The use of earthing spring 103-911 is advisable in cases where the earth has to be fetched from an earth test point located on the board.

Fig. 2.3-9 Probe adapter

Specially selected test points are designed for fitting the probe adapter, e.g. on sampling flip-flop IC 711, clock: v-v_a; DS^+: u-u_a.

1) Do not use an earthing plate with the following types, as Pin 1 carries a signal:
MC 10 124
MC 10 125
MC 10 186

2.3.1.2 Making measurements on SMD PCBs

Never make measurements on a SMD by touching the test probe directly onto the component. Use the PCB tracks, test points or plated-through holes as contact points instead. If you are using a test probe with a sprung tip, the solder joints can also be used (see figure 2.3-10).

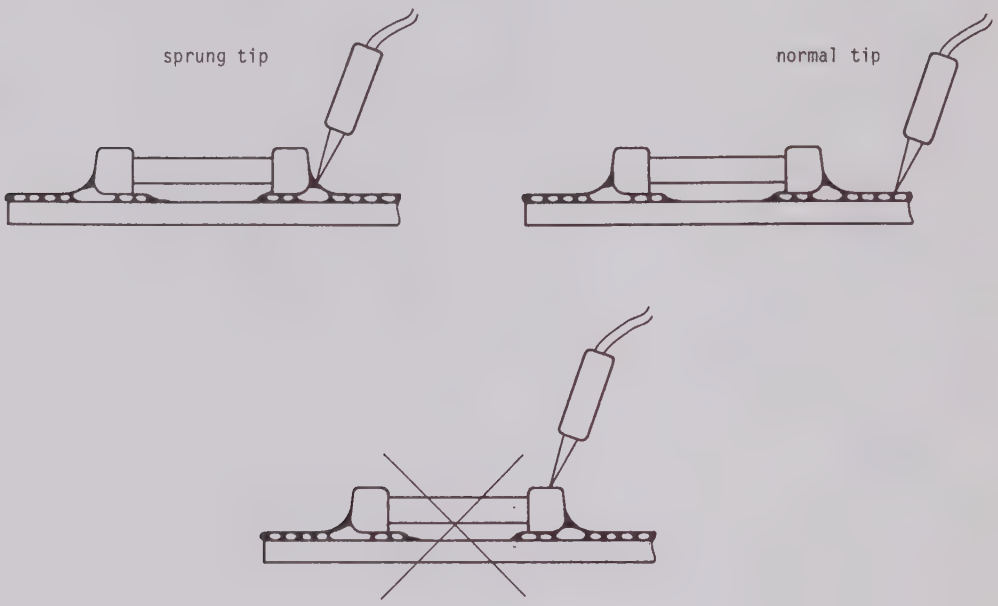


Figure 2.3-10 Making measurements on SMDs

2.3.2 SIGNATURE ANALYSIS

A signature analyzer (e.g. hp 5004A/5005A/5006A) can be used for unambiguous and simple checking of digital signal strings of any desired length. Constant signatures are obtained on the lines to be tested if defined and repeatable bit patterns are present in relation to a time window (= START/STOP frame). The bit stream to be measured is sampled via a probe in sychrony with the clock of the unit under test (UUT). If the signature analyzer has a qualifier input, the bit stream can be switched through it, e.g. by chip selection of an EPROM. In this case, the bit stream is then only analyzed within this "window". The resultant bit string is then compressed into a 4-digit display by a process of data compression. The signature analyzer has a built-in 16-bit shift register with feed-back for data compression, into which the data are read.

Transfer to the shift register is dependent on the bit combination in the feed-back circuit of the register at the time in question (see Fig. 2.3-11). The shift register can assume a total of 216 (or 65536) possible status combinations via a correspondingly long data stream.

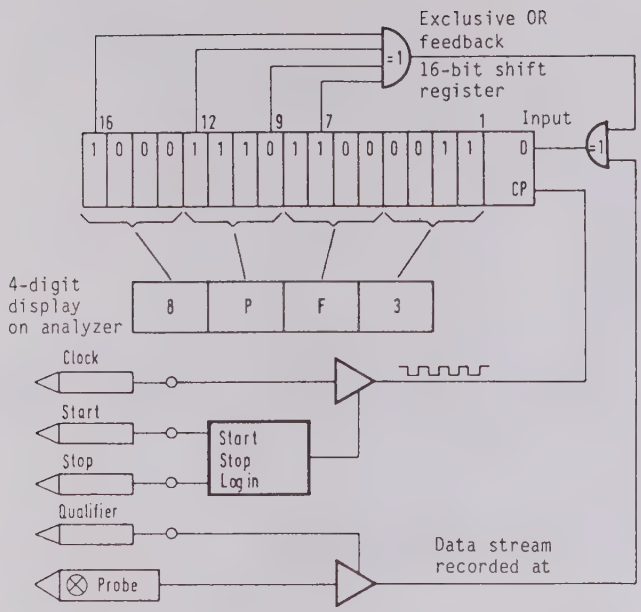


Fig. 2.3-11 Elementary circuit diagram of a signature analyzer

This status combination is then decoded, shown in pseudo-hexadecimal form via four 7-segment displays and thus becomes a signature.

This signature now represents the characteristic activitity at this circuitry point for a precisely defined period. Any change (e.g. a missing or additional bit, or a time offset in relation to the clock signal) will produce a different signature, thus indicating a fault.

The CLOCK signal used is a signal fulfilling the time conditions, RD or WR for the microprocessor. The timing of the CLOCK, DATA, START and STOP signals must be correct, since unstable signatures otherwise occur. Similarly, this timing cannot be guaranteed if signature analyzers other than those recommended by us are used, since they have different input circuits. Consequently, the signals may deviate from the expected results in these cases.
Two frequently occurring signatures need brief explanation:
The signature of the ØV line is always 0000, irrespective of the START/STOP frame. The signature of the +5V line is referred to as the "FRAME SIGNATURE". The frame signature shows whether the START/STOP frame is correctly connected and whether the edges for the START/STOP frame are correct. In addition, it may be assumed that the microprocessor is working.
If the frame signature occurs on an address or data line, this means a short-circuit against the supply voltage; the signature 0000 indicates a similar short-circuit, but to earth. If two address or data lines have the same signature, this is most probably due to a short caused by the lines touching.
In order to obtain meaningful signatures for the RAM and/or I/O area, verifiable contents must first be written into the RAM and the I/O ports then addressed periodically. This can only be done by a program, the so-called stimulus. Such programs can be called up via a switch, for example.

2.3.3 MONITOR FUNCTIONS

The assemblies in this measuring instrument are mainly microcomputer-controlled.
The instrument has monitor software to facilitate or enable troubleshooting.
This software contains the so-called WORIS functions.

-W: (Write) Write to memory location
-O: (OUT) Output to a gate
-R: (Read) Read memory location
-I: (IN) Input from a gate
-S: (Start) Start of a program or output of a complete set of parameters (e.g. on the SPM-15).

Section 6 describes how to enter the Monitor Mode in more detail.
Depending on the type of software, the monitor functions can be controlled via the front panel keyboard and/or with the external monitor control section "MONEX". The instrument-specific connection of the MONEX is described in Section 2.3.4.

2.3.3.1 Description of the basic functions of the monitor software

A command consists of
- a header W:, O:, R:, I: or S:,
- a 4-digit address field in hexadecimal notation,
- possibly a 2-digit data field (depending on command) in hexadecimal notation.

The command is entered by pressing the corresponding keys.

/CLR/ key:
The /CLR/ key can be used to delete the last character entered.

/EX/ key:
The command is executed by pressing the /EX/ key.
If the instrument has no CLR or EX keys, keys with similar designations are used for these functions, e.g. /ENTER/ instead of /EX/.

/MON/ key: (only on the external control section "MONEX")
Initialization of the monitor software. Pressing this key re-initializes the software, thus making it ready for operation.

The "W:" command: Write to a memory location

Syntax:	W:xyzt.dd xyzt: Address of the memory location (hexadecimal) dd: Data byte (hexadecimal)
Effect:	The data byte dd is stored at address xyzt after pressing the EX key. Execution of the command is confirmed by the display: "W:xyzt.dd!"
Abbreviated entry	The address and the data byte may be entered with less than 4 or 2 digits. In this case, they are padded with leading zeros (e.g. 3 is interpreted as 0003 or 03, respectively).

If a number key (0...F) is pressed after operating the /EX/ key, the address is automatically increased by one and the number accepted as the first digit of the data byte. The second digit of the data byte is then entered in the usual manner.

If the /EX/ key is pressed twice in succession, the address is automatically increased by one and the same data byte stored at this memory location.

If the /./ key is pressed after operating the /EX/ key, the address remains unchanged. The data field is cleared and ready for entry of the data byte.

The "O:" command: Output to an output gate

Syntax:	O:xy.dd xy: Address of the output gate (hexadecimal) dd: Data byte (hexadecimal)
Effect:	The data byte dd is output to the gate xy after pressing the EX key. Execution of the command is confirmed by the display: "O:xy.dd!"
Abbreviated entry	The address and the data byte may be entered with less than two digits. In this case, they are padded with leading zeros (e.g. 3 is interpreted as 03).

If a number key (0...F) is pressed after operating the /EX/ key, the address is automatically increased by one and the number accepted as the first digit of the data byte. The second digit of the data byte is then entered in the usual manner.
If the /EX/ key is pressed twice in succession, the address is automatically increased by one and the same data byte output to this gate.

If the /./ key is pressed after operating the /EX/ key, the address remains unchanged. The data field is cleared and ready for entry of the data byte.

The "R:" command: Read memory location

Syntax:	R:xyzt xyzt: Address of the memory location (hexadecimal)
Effect:	The data byte dd is read from the address xyzt after pressing the EX key. Execution of the command is confirmed by the display: "R:xyzt.dd!"
Abbreviated entry:	The address may be entered with less than 4 digits. In this case, it is padded with leading zeros (e.g. 3 is interpreted as 0003).

If the /EX/ key is pressed twice in succession, the address is automatically increased by one and its contents read out. If the /./ key is pressed after operating the /EX/ key, the address remains unchanged. The data field is cleared. The address contents are read out again after pressing the /EX/ key.

The "I:" command: Input from an input gate

Syntax:	I:xy xy: Address of the input gate (hexadecimal)
Effect:	The contents of gate xy are read out after pressing the EX key. Execution of the command is confirmed by the display: "I:xy.dd!"
Abbreviated entry:	The address may be entered with less than 2 digits. In this case, it is padded with leading zeros (e.g. 3 is interpreted as 03).

If the /EX/ key is pressed twice in succession, the address is automatically increased by one and the corresponding gate contents read. If the /./ key is pressed after operating the /EX/ key, the address remains unchanged. The data field is cleared. The gate contents can be read again by pressing the /EX/ key.

The "S:" command: Starting a program

Syntax:	S:xyzt xyzt: Start address of the program (hexadecimal)
Effect:	The program with the address xyzt is called up after pressing the EX key. Execution of the command is confirmed by the display: "S:xyzt!"
Abbreviated entry:	The address may be entered with less than 4 digits. In this case, it is padded with leading zeros (e.g. 3 is interpreted as 0003).

If the /EX/ key is pressed twice in succession, the same program is called up again.

The "W:" function can be used to write a program into the free data area for subsequent starting with the "S:" function. Such a program may be, for example, a repeating INPUT function.

Notes:

In order to exit the endless loop, the interrupts must be free. The endless loop can be exited by pressing the "MON" key, which re-initializes the monitor software.
The command EI = ØFBH (EI = Enable Interrupt) must be inserted into the endless loop.
If the program is an endless loop, and if it is started repeatedly with the function "S:", the return address is saved at each interrupt by the "S:" key, but never restored. The stack overflows. Consequently, the stack must be re-initialized at the start of an endless program.

2.3.3.2 Basic configuration of the external control section MONEX

The external monitor control section MONEX (including adapter for CPU) has the following characteristics:

1. The keyboard interrupt of the MONEX can optionally be connected to RST 5.5, RST 6.5 or RST 7.5 via the software.
   In the standard version, the keyboard interrupt of the MONEX is connected to RST 6.5 and ORed with the interrupt of the instrument keyboard, although this assignment can be changed in accordance with instrument-specific requirements.

   The MONEX front panel has one green LED for each RST. A flashing LED means that the MONEX keyboard interrupt is connected to the RST in question and that the MONEX keyboard is free (MONEX keyboard interrupt flip-flop reset).

   If the MONEX keyboard interrupt flip-flop is set, i.e. if the MONEX keyboard interrupt is not processed immediately for any reason whatsoever (e.g. in the event of a fault), the green LED lights up constantly.

2. The instrument interrupts are connected from the card rack via the adapter through to the CPU via DIL switch S1 and the adapter. This means that interrupt-controlled instrument functions can also be operated from the MONEX.

   If unwanted interrupts from the card rack are present in MONEX mode, they can be disconnected with DIL switches S 1/1, S 1/2 and S 1/3 (see Fig. 2.3-12).

S 1/1	RST 5.5	ON
S 1/2	RST 6.5	ON
S 1/3	RST 7.5	ON
S 1/4	IORD	OFF
S 1/5	SOD	OFF
S 1/6		

ON/(OFF) RST signal from card rack (not) connected through to CPU

OFF: IORD signal not linked with MONEX addresses.

OFF: MONEX addresses not linked with SOD signal.

Fig. 2.3-12 DIL switch S1 on the adapter board, basic settings

Note on S 1/4: This instrument has incomplete gate address decoding. If the addresses FØ ... FF reserved for the MONEX are selected, additional drivers are activated on the I/O bus and a bus conflict occurs. Thus, if MONEX gate addresses FØ ... FF are selected, the IORD signal on the adapter must be interrupted with S 1/4. The normal setting is S 1/4 OFF, i.e. IORD is connected through from the CPU board to the card rack.

Note on S 1/5: In the case of instruments with address expansion via the SOD line (PRA-1), the adapter version with SOD link must be used (with S 1/5). If S 1/5 is closed, the MONEX addresses are inhibited when SOD = H.

The MONEX front panel includes one red LED for each interrupt; the corresponding LED lights up whenever an interrupt is received from the card rack. However, a short pulse is not visible, since the LEDs are only connected to the RST lines via drivers. These LEDs also light up if the instrument interrupts are not connected through to the CPU-2 board (S 1/1 ... S 1/3 set to OFF).

2.3.3.3 Service EPROM

A "Service EPROM" has been designed for fully developed instruments with the CPU board*, which contains not only the monitor software, but also all the instrument-independent self-test and repair programs. If EPROMØ of the CPU-2 board is replaced with the "Service EPROM", the monitor functions and the test programs can be called up in the same way on all instruments using the external monitor control section MONEX. Naturally, the basic instrument is then no longer functional.

Refer to Section 2.3.4 for operation of the monitor functions using the external control section MONEX.

The initialization routine after switching on the instrument includes a short self-test, during which EPROMØ and the I/O bus of the CPU-2 board are tested. "000" appears on the MONEX display if no faults are found.

Start addresses of the test programs:

120H	EPROMØ test
125H	RAM test, non-destructive (excl. arithmetic processor Am9511)
130H	RAM test, non-destructive (incl. arithmetic processor Am9511)
135H	I/O bus test
140H	Test of arithmetic processor Am9511
145H	Test of screen control board
150H	Test of the IEC bus interface board

*: The software is in a 32K EPROM instead of an 8K EPROM for the CPU-2A and CPU-2B.

Error detection:

Errors detected appear on the display in clear text.
In the RAM test, the error is defined more closely, as follows:

Non-destructive RAM-Test	00H:	Error in cell test in RAM 0
	01H:	Error in cell test in RAM 1
	02H:	Error in cell test in RAM 2
	03H:	Error in cell test in RAM 3
	10H:	Addressing error in RAM 0
	11H:	Addressing error in RAM 1
	12H:	Addressing error in RAM 2
	13H:	Addressing error in RAM 3
	20H:	Addressing error (address lines A11 and A12)

Note: All 4 RAMs must be fitted on the CPU-2 board.

2.3.4 ADAPTATION AND NOTES ON USING THE EXTERNAL MONEX WITH THE PJM-4

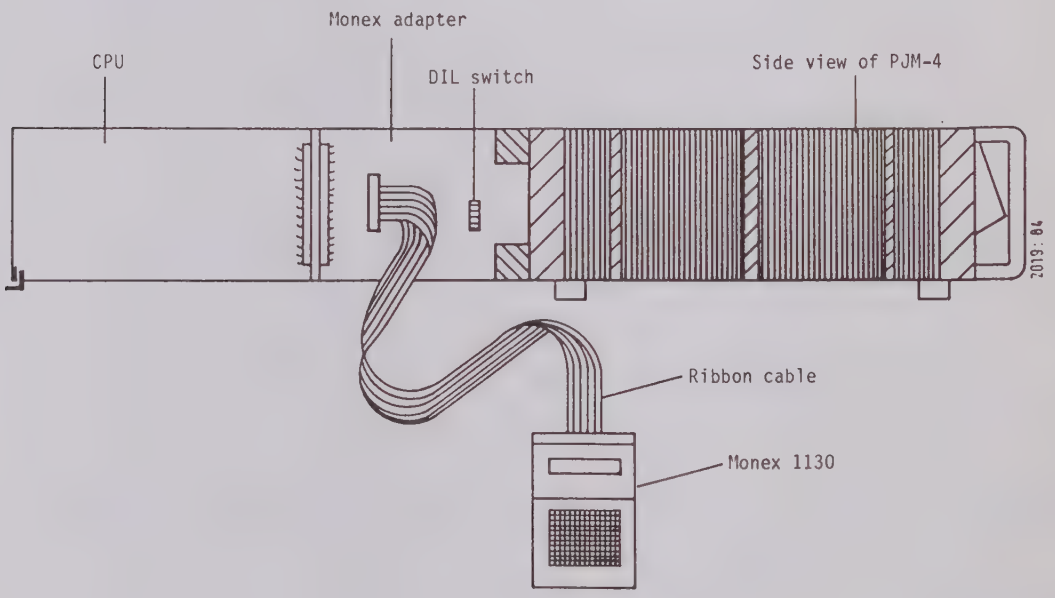


Fig. 2.3-13 Adapting the MONEX 1130 to the PJM-4

Note:

Troubleshooting in relation to use of the MONEX presupposes a good knowledge of programming in machine language.

The software for operation with the external MONEX control section is integrated into the PJM-4. The MONEX control section is connected between CPU-2A and the card rack by means of its adapter.

Switches on the MONEX adapter

S 1/1 RST 5.5 (keyboard)

Open : Keyboard interrupt from instrument front panel disabled, PJM-4 keyboard disabled.

Closed: Keyboard interrupt enabled:
PJM-4 and MONEX keyboards both enabled. (Keyboard interrupt of MONEX switched to RST 5.5 by PJM-4 at initialization).

S 1/2 RST 6.5 (100 ms meas. interrupt)

Open : 100 ms measuring interrupt disabled:
Important for input section and AF section tests if steady-state settings are to be made.

Closed: Measuring interrupt enabled:
Divider setting, input section,
Lock-in control,
Divider control, jitter measuring section
are controlled automatically.

S 1/3 RST 7.5 (IEC bus)

Open : IEC bus interrupt disconnected

Closed: IEC bus interrupt enabled

S 1/4 Address decoding FØH ... FFH

Any setting:
In the PJM-4, the address range FØH ... FFH is exclusively reserved for the MONEX.

S 1/5 I/O address range switching by means of SOD

Open setting:
In the PJM-4, the SOD line is not used for switching the address range.

Application example with MONEX

Switch settings on MONEX adapter:
S 1/1 ... S 1/5 open

```
        O : 65 . FC         "EX"
```

TIME display on front panel lights up.

```
        O : 65 . FF         "EX"
```

TIME display on front panel goes out.

```
        S : 143             "EX"
```

The cyclic display test is started (also see Section 9.3.5).

2.4 SOLDERING INSTRUCTIONS

2.4.1 SOLDERING ON CIRCUIT BOARDS OF PLATED-THROUGH DESIGN

The use of thin soldering tin with little flux is recommended, e.g. the standard solder "ELSOLD L-Sn 60 Pb Cu 2 C3 F-Sw 32; 3,5%" from Bleiwerke Goslar GmbH & Co.
The following points must also be kept in mind:

- The soldering time should not exceed 1 to 3 seconds.
- The best soldering temperature for the above-mentioned solder is 240 to 280 °C.
- In this case, the soldering iron temperature should be about 325 ± 5 °C.
- Broader soldering tips must be used for soldering points with a high heat requirement. If this measure proves inadequate, a more powerful soldering iron must be used (70 W, 100 W).

  Note: The soldering iron temperature must not be increased to cover a higher heat requirement! This is because temperatures in excess of 300 °C cause severe oxidation of the solder; also, the flux loses some of its activity at temperatures above 280 °C.
  In extreme circumstances, a "cold solder joint" may still result.
- Avoid flux splashes on switch contact points.
- When soldering on switch contacts or other electromechanical components, try to prevent flux getting onto contacts.

Note on desoldering components with numerous connections:

The best method by far is to remove the solder of each individual connecting pin by suction using special-purpose desoldering equipment. Move the pin gently back and forth while desoldering, to check that each individual connection is free. Do not use force!
Through-platings are sensitive to tensile stresses during soldering!
In the case of dual in-line components, the stress on the circuit board can be reduced considerably by cutting the connections on the component side and desoldering the individual connections.

2.4.2 SMD PCB SOLDERING AND REPAIR INSTRUCTIONS

2.4.2.1 Introduction

Repair and soldering work on pcbs fitted with SMDs requires the use of special tools and techniques to ensure the reliability of the completed job, so it is important that such work is only carried out by persons familiar with these techniques. Details of the specialist equipment required are found in section 1.3 (Tools and equipment) of this manual.

In particular, the guidelines given in sections 2.3.1, 2.4.2.2 and 2.4.2.3 should be observed, otherwise damage to components and pcbs may occur. If you do not have the necessary facilities for carrying out such work, we suggest that you simply exchange the defective pcb or module for a new one.

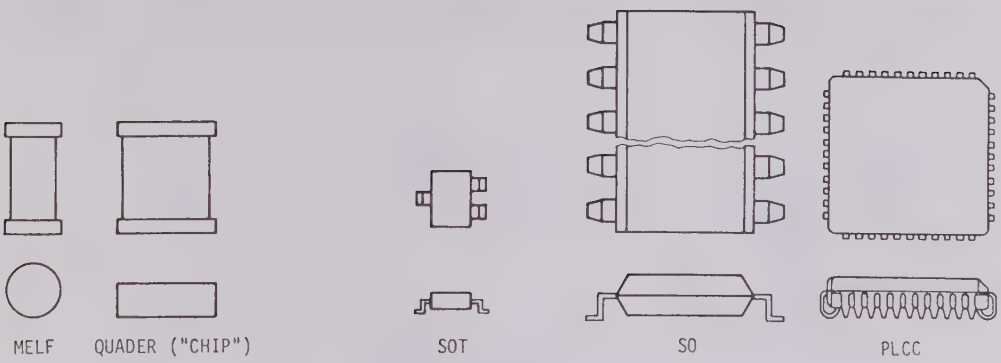


Figure 2.4-1 Outline drawings of SMDs

2.4.2.2 Instructions for handling SMDs

Surface-mounted devices are easily damaged, so care must be excercised when handling them. Traces of grease (e.g. fingerprints) are sufficient to prevent solder from flowing properly. Contact points are often closely spaced, requiring utmost precision when soldering to avoid short circuits.

The following guidelines should be observed:

- Always use tools and equipment specially designed for working with SMDs (e.g. special tweezers, etc.). Refer to section 1.3 of this manual for more details.
- As component values are not normally printed on SMDs, to avoid confusion keep the devices in their original packing until required.
- Since the contact surfaces must be kept scrupulously clean, always use tweezers for handling components, grip the body of the component only. The contacts should only be touched by the special test clips used when measuring component values.
- If you accidentally drop a SMD, throw it away as it is quite likely that hairline cracks have occurred, particularly in the larger types of SMD.

2.4.2.3 SMD soldering and repair instructions

These instructions apply to SMDs only. Faulty pcb tracks can be repaired using conventional techniques.

The main point to bear in mind when repairing SMD pcbs is that these are much more easily damaged than normal pcbs. In particular, solder pads are easily damaged. If this occurs, the pcb can only be repaired by the use of special bonding methods (see under repairing damaged solder pads).

The following guidelines should be observed:

- Soldering iron tip temperature should be 290 °C (max. 300 °C).
- If hot gas techniques are used for soldering, the gas temperature should be 400 °C.
- Soldering times should be kept as short as possible, but in any case not more than 3 seconds.
- When desoldering SMDs, twist the component slightly once the solder has melted and then lift it off (see figure 2.4-2).

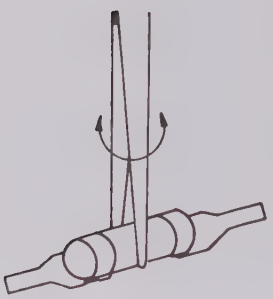


Figure 2.4-2 Desoldering a SMD

- If you accidentally remove the wrong component, don't re-use it; replace it with a new one.
- Flux (type FSW-32), solder paste (e.g. Heraeus SC 3300 RMA or 3301 RMA) and thin-gauge solder (0.3 to 0.6 mm diameter, 60/40 Sn(Pb alloy) may be used as required.

Desoldering

a) MELF and chip type SMDs (see figure 2.4-1):
Use special soldering tweezers or hot gas soldering equipment; if these items are not available, a soldering iron fitted with a fork bit can be used. After removing the component, remove excess solder from the pads with a fine tipped desoldering tool.

b) SOT type components (less than 6 pins):
Use hot gas equipment or cut through the pins as described under (c) below.

c) SO and PLCC type components (more than 6 pins):
Use hot gas equipment capable of heating all the connections simultaneously, otherwise damage to the pcb is inevitable. If such equipment is not available, the pins can be cut through close to the component using an IC end cutter (very fine pointed side cutter). The remains of the pins should then be desoldered carefully and the solder pads sucked clean.

Soldering

a) MELF and chip type components:
Use hot gas equipment or a soldering iron fitted with a fork bit. It is important that both solder joints are liquid at the same time.

b) Multipin components (SOT, SO, PLCC):
Use a miniature soldering iron or hot gas equipment. Solder IC pins on alternate sides in a diagonal pattern to avoid overheating the component.

After completing soldering, examine the solder surfaces under a magnifying glass to ensure that the joints are satisfactory (i.e. absence of solder whiskers, cracks, dry joints, solder blobs; joints should be even and uniformly shiny). Also check that the SMD is correctly positioned.

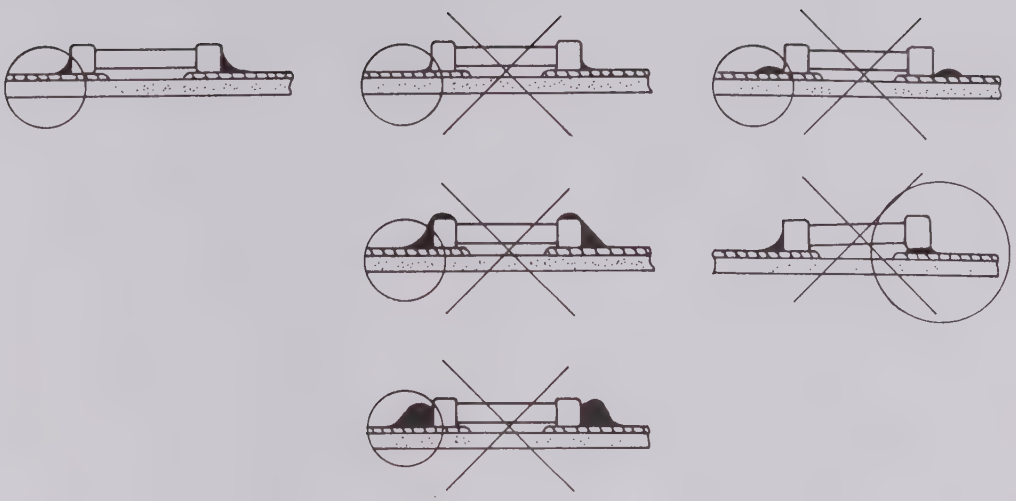


Figure 2.4-3 Illustrations of good and bad solder joints

Repairing damaged solder pads

Use 60/40 Sn/Pb alloy solder, 0.6 mm or 0.3 mm diameter and FSW-32 flux for all repair work.

For multipin SMDs (IC, SOT, PLCC etc.):

First solder the component in position using the undamaged solder pads. Then repair the damaged pad(s) as follows:
Connect one end of a length of 0.2 mm dia. enamelled wire to the pin of the SMD. Connect the other end to the nearest correct contact point. A plated-through hole is best for this purpose, or else the connecting pin of the next SMD in the circuit.

For pinless SMDs (MELF, mini MELF resistors, diodes, tantalum and multilayer capacitors, chip components, etc.):

1) Connect the SMD in the usual way to the good solder pad. Connect a length of 0.6 mm diameter wire (insulated if necessary) to the other SMD contact and solder the other end of the wire to an appropriate plated-through hole or SMD contact. The length of the wire should be less than 10 mm.

2) If method 1 cannot be used, the SMD must be held in place with adhesive:
   - Put a spot of adhesive (e.g. Heraeus PD 86 0002) on the pcb
   - Place the SMD in position on the pcb
     Allow the adhesive to cure (100 °C for 20 min.)
   - Connect 0.2 mm diameter wire to the SMD and route to an appropriate connecting point.

If no free contact points are available near the point of repair, or if connections have to be kept as short as possible, it may be possible to carefully remove the solder resist and oxide coating from a wide pcb track and solder the wire to this point.

3 MECHANICAL DESIGN, MAINTENANCE 3-1

3.1 Instrument data 3-1
3.1.1 Identification of the software version 3-1

3.2 Location of assemblies 3-2

3.3 Assembly instructions 3-7
3.3.1 Assembly instructions, overall instruments 3-7
3.3.1.1 Dismantling the instrument; opening the instrument 3-7
3.3.1.2 Shielding troughs and frames 3-8
3.3.1.3 Replacing operating elements (key caps and their spring inserts 3-9
3.3.2 Assembly instructions, assemblies 3-11
3.3.2.1 Power supply unit (modular power supply unit 3-11
3.3.2.2 Dismantling the plug-in cards 3-11
3.3.2.3 Display/keyboard 3-12
3.3.2.4 "RF block" chassis 3-13
3.3.2.5 (14) RF control [2019-F] 3-13

3.4 Installing options 3-14
3.4.1 <Option> (4) code error card 2 (2019/00.01) 3-14
3.4.2 <Option> additional bit rates (2019/00.11 3-14

3.5 Maintenance work 3-15
3.5.1 Storage batteries (Series A, Series B...) 3-15

3.6 Cleaning work 3-15

3 MECHANICAL DESIGN, MAINTENANCE

3.1 INSTRUMENT DATA

The following instrument data are required for enquiries, spare parts orders and to establish whether this Service Manual belongs to the instrument to be repaired:

Type designation, designation of the specific model, software version number, options installed, Series index and instrument number.

Fig. 3.1-1 shows where the individual data items are to be found.

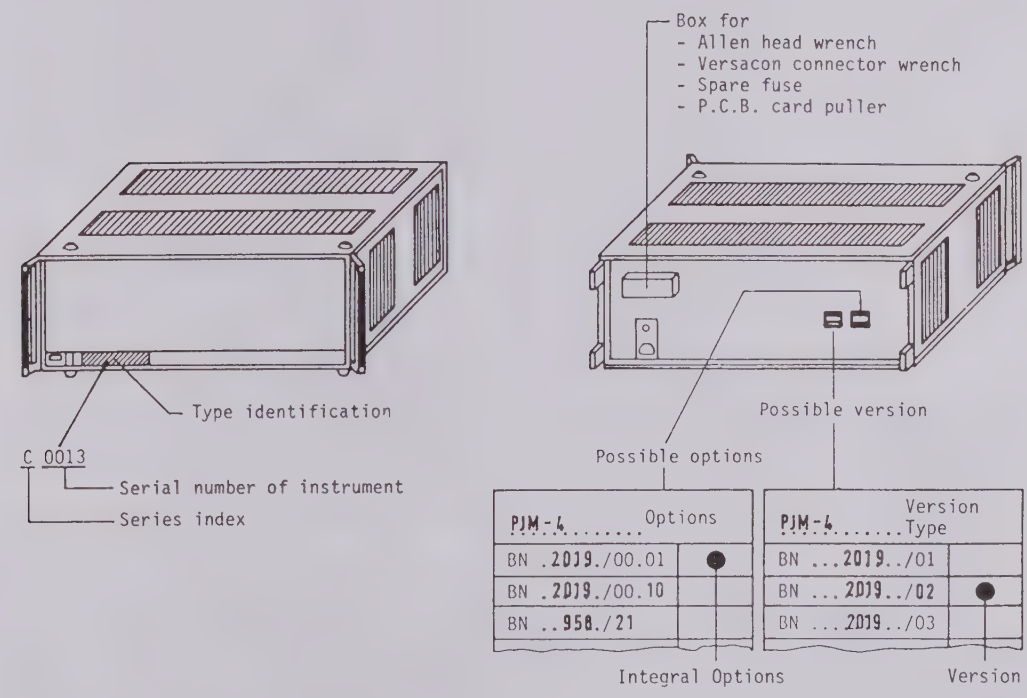


Fig. 3.1-1 Instrument data

3.1.1 IDENTIFICATION OF THE SOFTWARE VERSION

The software version is identified

- via the BV of the signature list (the signature list is affixed inside the instrument)
- by calling up the instrument-specific test menus (see Section 9.3.1)

If the software is subsequently upgraded, it must be ensured that the signature list is supplemented or replaced.

3.2 LOCATION OF ASSEMBLIES

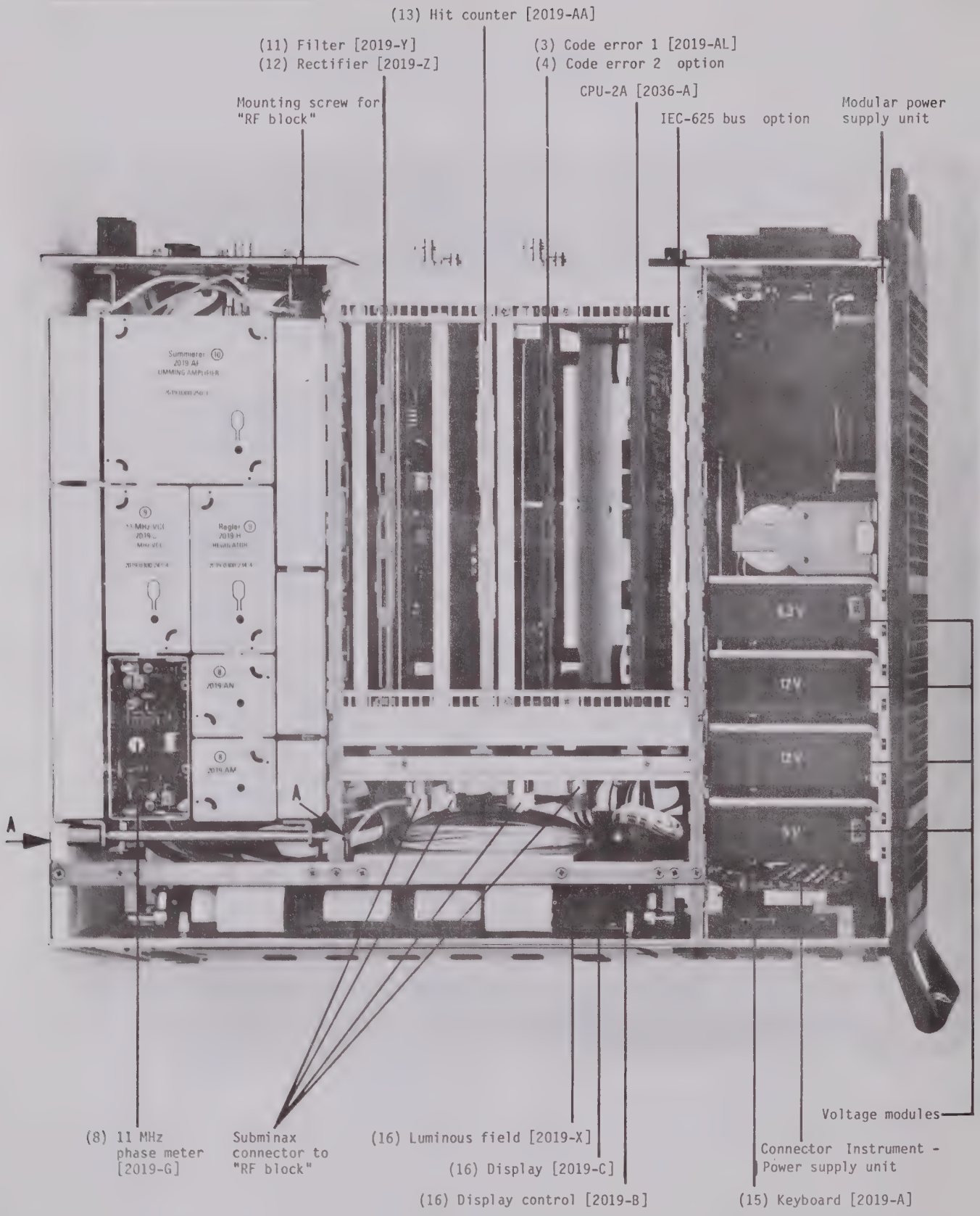


Fig. 3.2-1 Top view of PJM-4

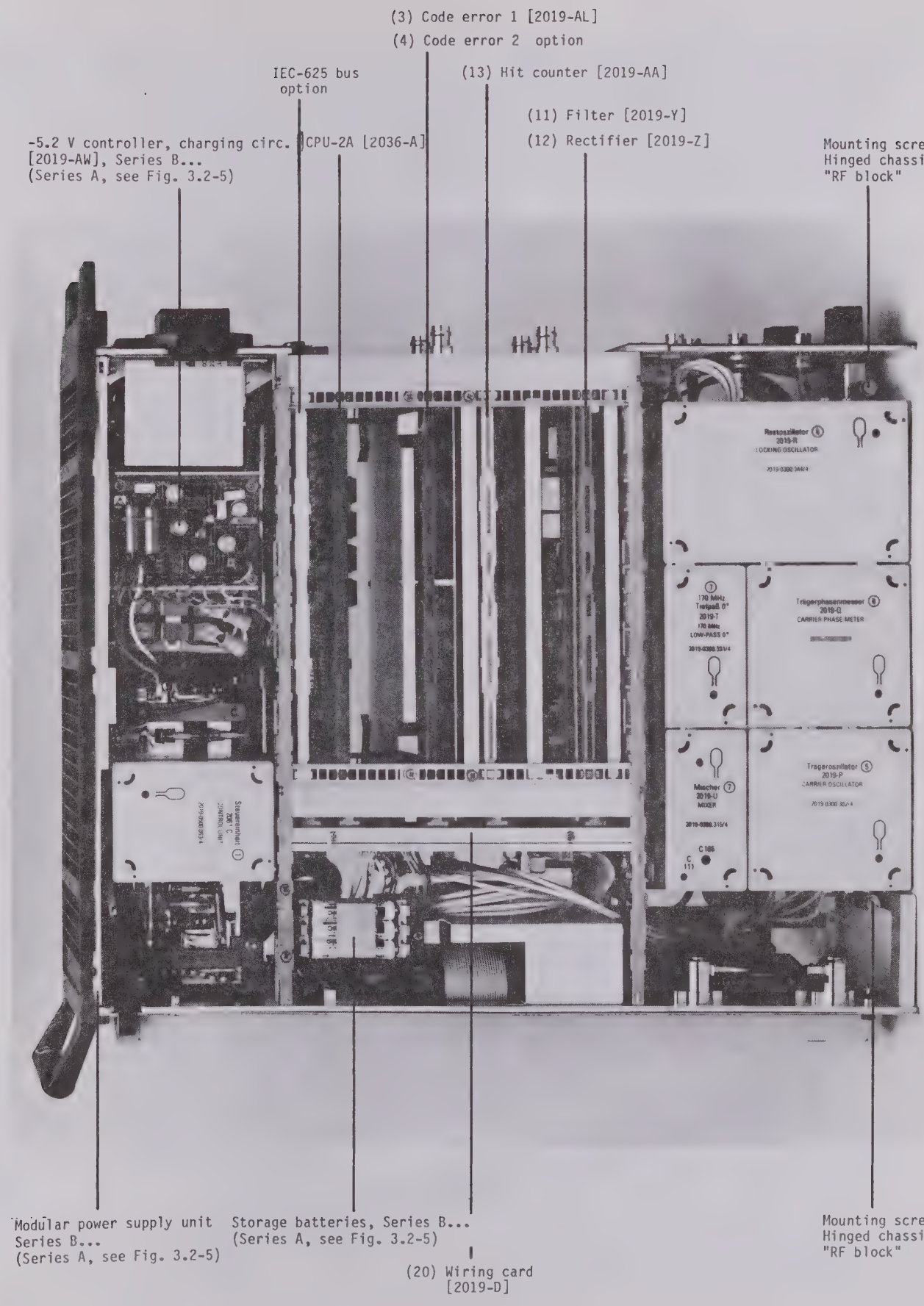


Fig. 3.2-2 PJM-4 from below, with power supply unit and storage batteries of Series B...

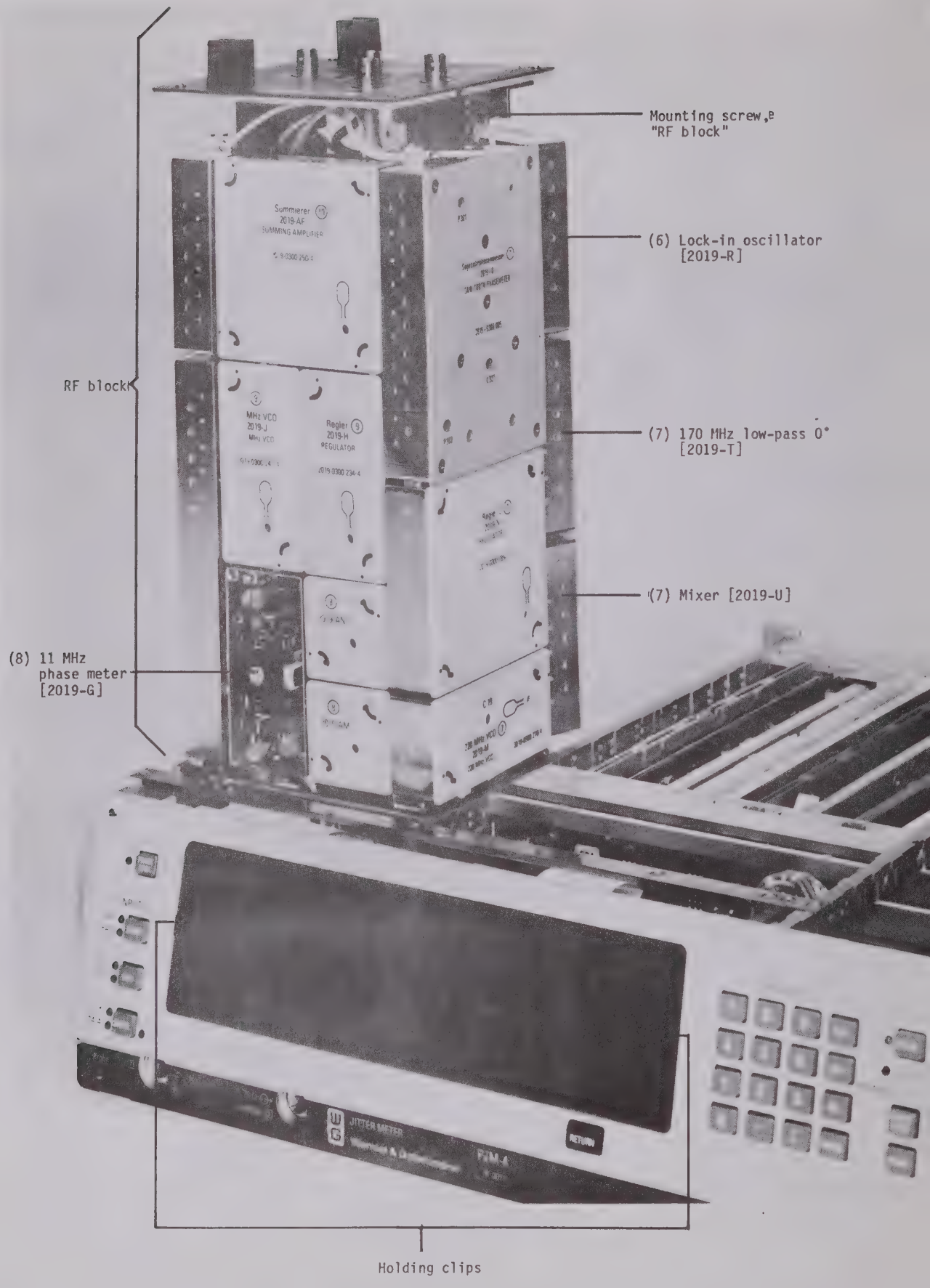


Fig. 3.2-3 "RF block" swung up

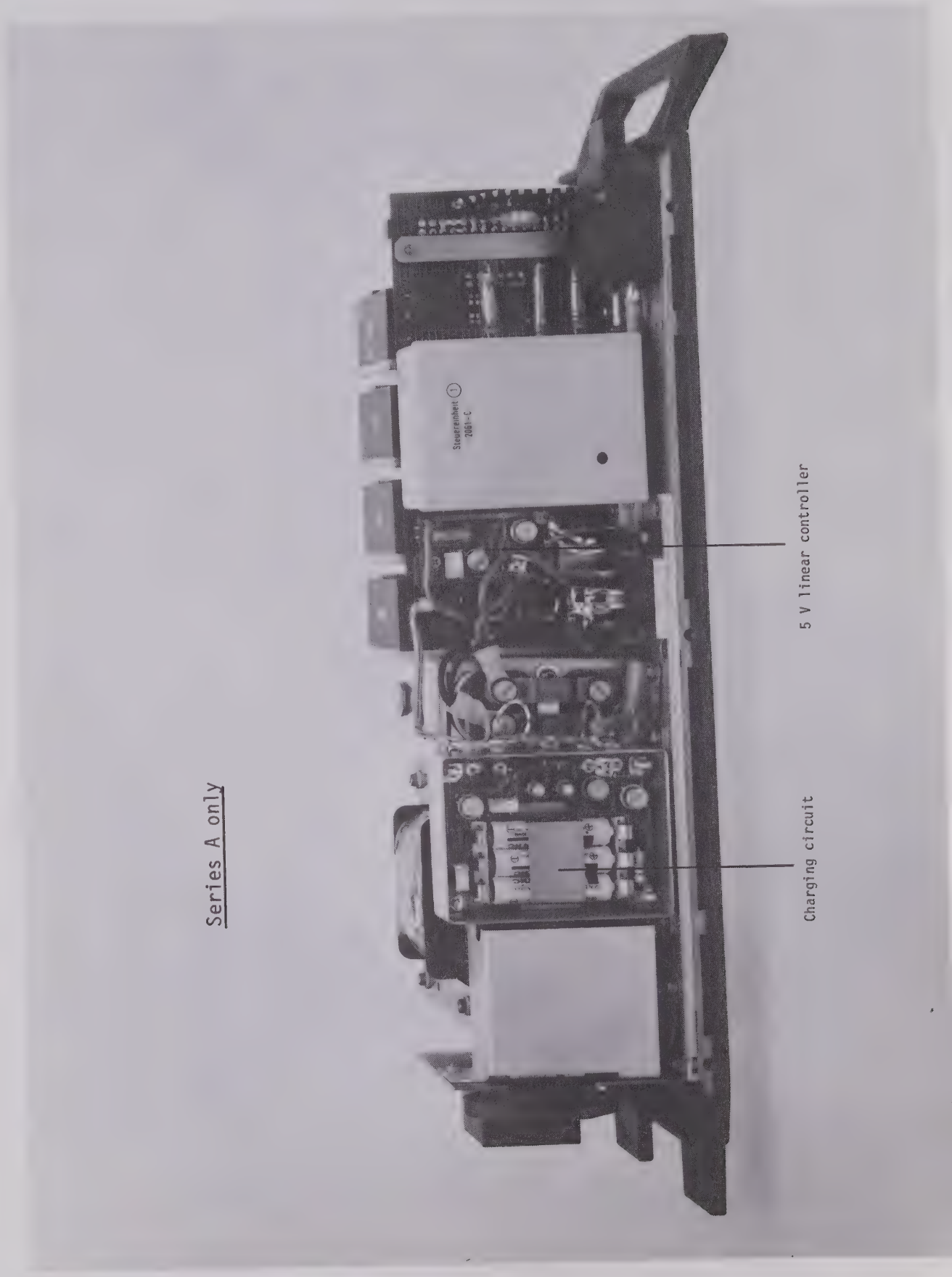


Fig. 3.2-5 Power supply unit, Series A

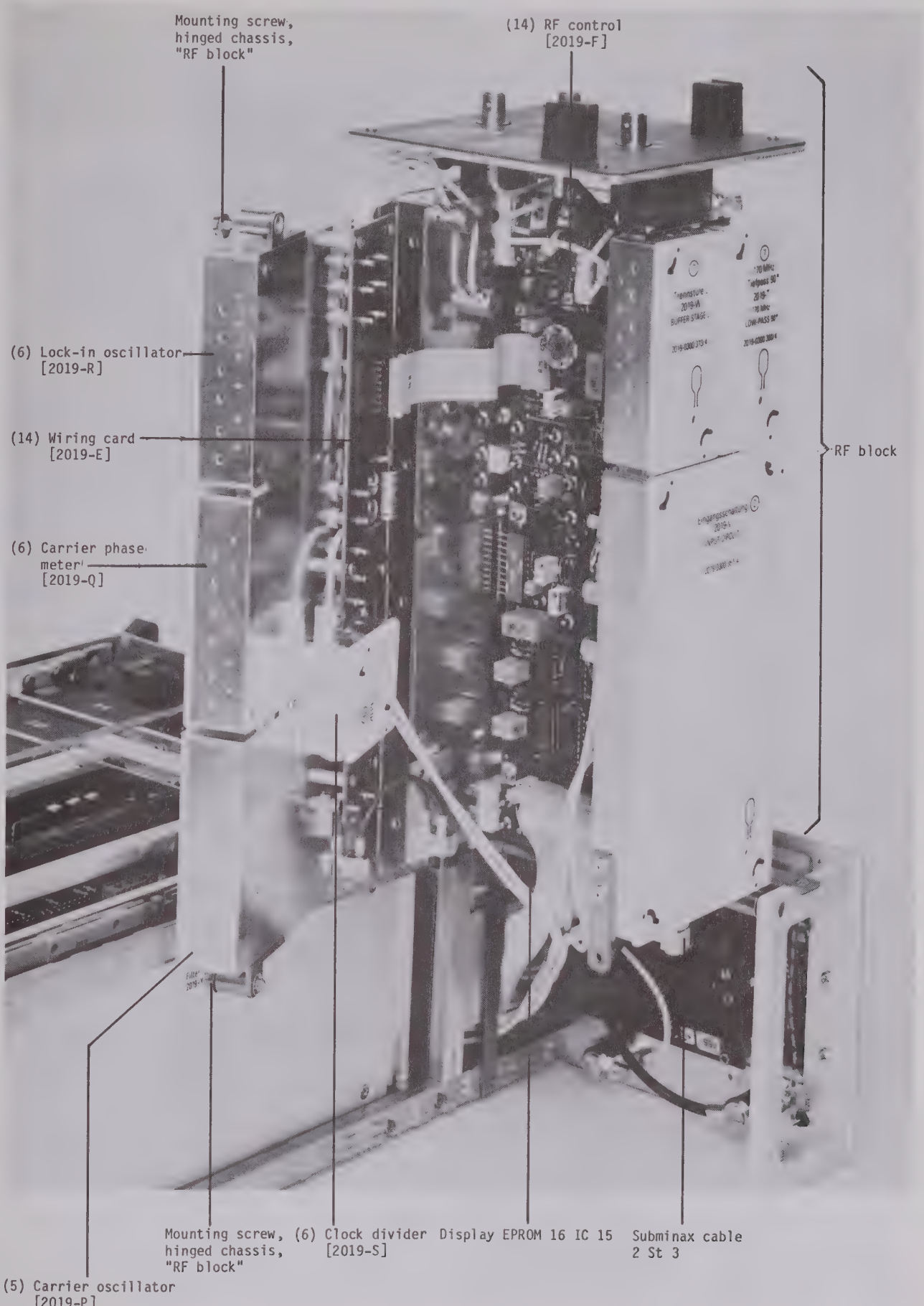


Fig. 3.2-4 "RF block" swung out

3.3 ASSEMBLY INSTRUCTIONS

3.3.1 ASSEMBLY INSTRUCTIONS, OVERALL INSTRUMENT

3.3.1.1 Dismantling the instrument; opening the instrument

The instrument can be lifted up and out of the housing after removing the 6 Allen screws at the top. The power supply unit remains in the housing. However, it is electrically connected to the instrument via a cable harness.

Tool:
Allen key, size SW 3
(see rear of instrument)

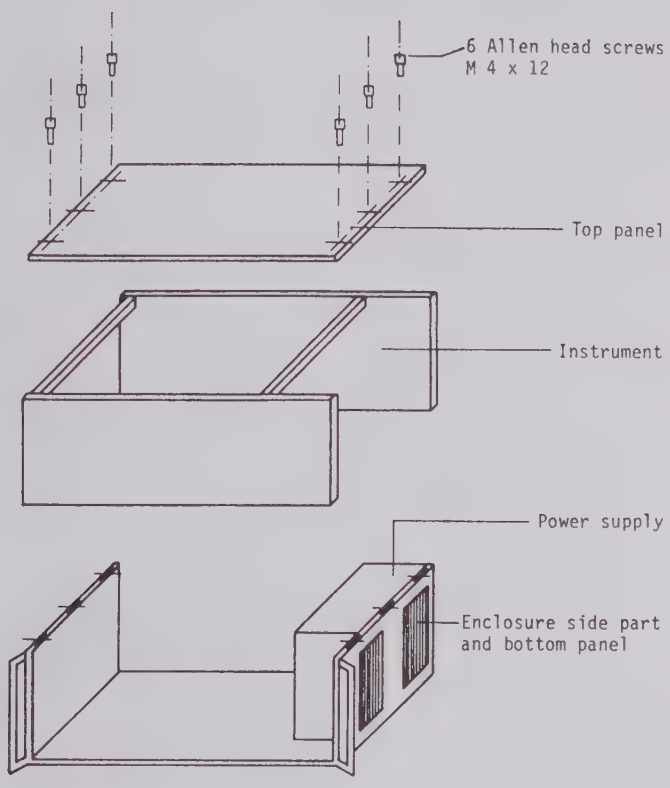


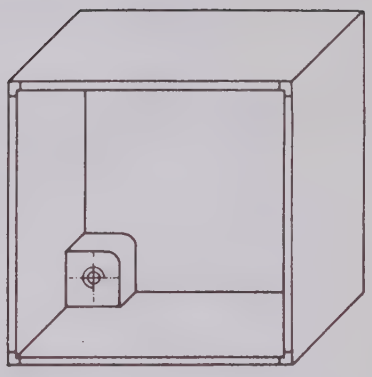
Fig. 3.3-1 Dismantling the instrument

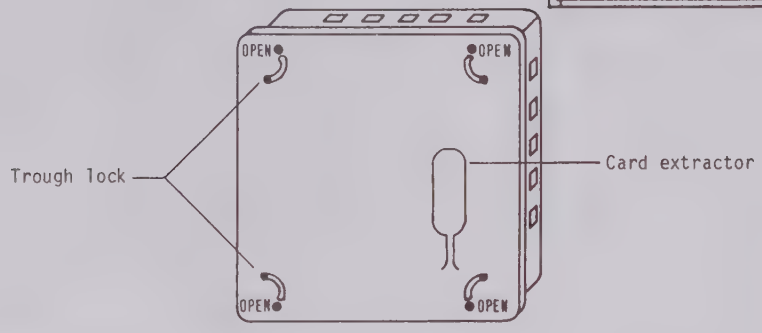
3.3.1.2 Shielding troughs and frames

Removing the covers from shielding troughs and frames

The covers are removed from the frames and troughs using the card extractor. Open the trough locks beforehand.

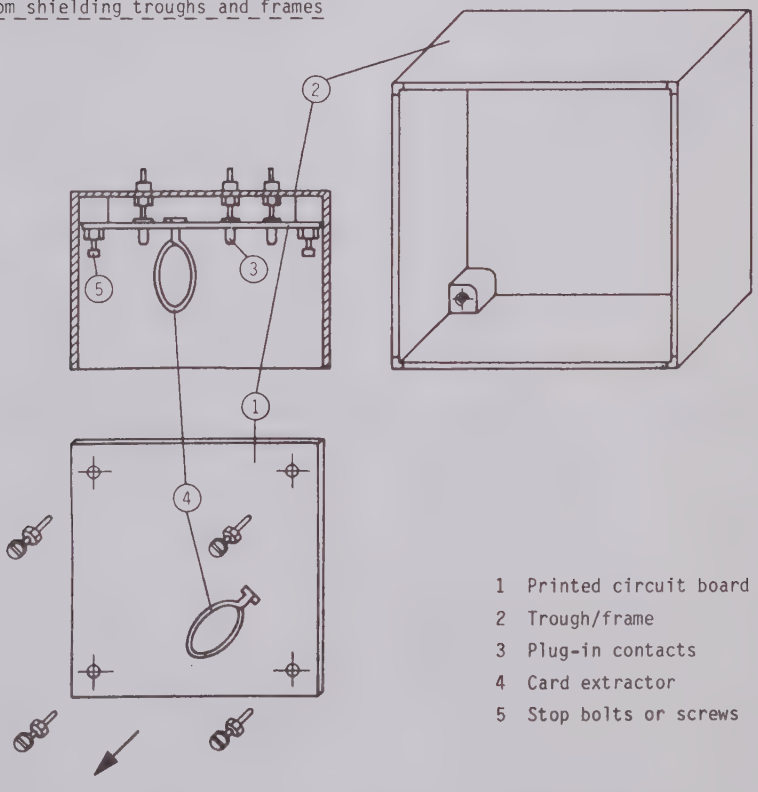
Proceed with caution when replacing a cover!
Rough handling could damage the thin prongs.





Removing the circuits from shielding troughs and frames

Section through the shielding



If supported appropriately, the board can be removed approximately parallel to its installation position. This helps to avoid bending of the prongs.

1 Printed circuit board
2 Trough/frame
3 Plug-in contacts
4 Card extractor
5 Stop bolts or screws

The stop bolts or socket head cap screws holding the printed circuit board must be removed, as must all chassis screws. Then pull out the board using the card extractor. When re-fitting, make sure not to skew the board in order to protect the contact pins.

Fig. 3.3-2 Shielding troughs and frames

3.3.1.3 Replacing operating elements (key caps and their spring inserts)

We recommend the following tools for replacing key springs* without dismantling the instrument:

- 1 special pliers, Order No. W-31
- 2 levers, Order No. W-32

* The springs of the keys from Messrs. Preh formerly used (recognizable by the black key housing) cannot be replaced.

Order No. for spare key springs: 30.230.01
Subject No. for complete spare key: 0000-7564.235

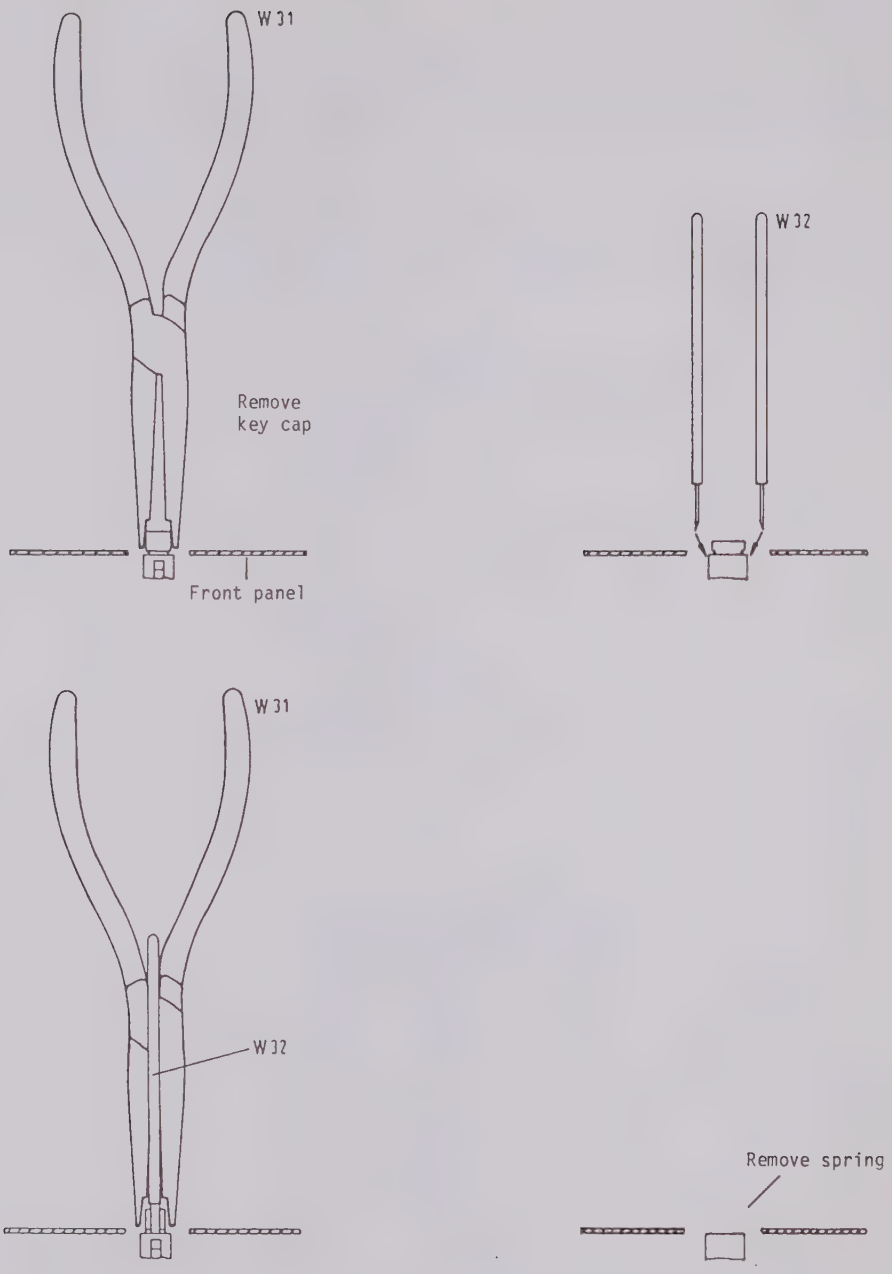


Fig. 3.3-3 Replacing key caps or spring inserts

3.3.2 ASSEMBLY INSTRUCTIONS, ASSEMBLIES

3.3.2.1 Power supply unit (modular power supply unit)

The power supply unit assembly comprises the following:

- Transformer unit
- Control unit
- Charging circuit
- DC/DC converter +5 V, +12 V, -12 V, -6.3 V
- 5.2 V linear controller
- Wiring card

Power supply unit assembly (Series A, Series B...)

Lift the instrument out of the housing in accordance with the assembly instructions in Section 3.3.1.1 and unplug the connector between housing and power supply unit.

Note: The power supply unit of a Series A instrument cannot simply be replaced by a Series B... power supply unit.

In Series A, the storage batteries and charging circuit are on a single board. The 5 V linear controller is located alongside the control section.
In Series B, the charging circuit and the 5 V linear controller are on a single board. The storage batteries are located outside the power supply unit.

Fig. 3.2-5 shows the power supply unit for Series A.
Fig. 3.2-2 shows the power supply unit from Series B onwards

DC/DC converter module

- Disconnect the power supply unit from the instrument, as described above.
- The DC/DC module can be separated from the wiring card after removing 3 Phillips screws.

  Note: When replacing the DC/DC converter, ensure that the newly fitted converter is compatible with the one replaced.

- The production version of the DC/DC converter is identified by a multi-digit number on the mounting bracket of the converter. Always state this number on enquiries and orders.

Also refer to the description of the DC/DC converter in the last part of Section 9.2.12.2 (additional functions).

3.3.2.2 Dismantling the plug-in cards

After removing the rear wall cover, the plug-in cards can be extracted and operated with the adapter card 901/00.11.

See Fig. 3.2-1 and Fig. 3.2-2 for the card locations.

Double card (3) Code error 1 [2019-A], (4) Code error 2 [Option]
- With option Code error 2 as double card

Double card (11) Filter [2019-Y], (12) Rectifier [2019-Z]
- (12) Rectifier mounted on (11) Filter board

3.3.2.3 Display/keyboard

Dismantling the complete front unit for replacement or troubleshooting

Remove the front panel.

See Fig. 3.3-4 for further dismantling steps.

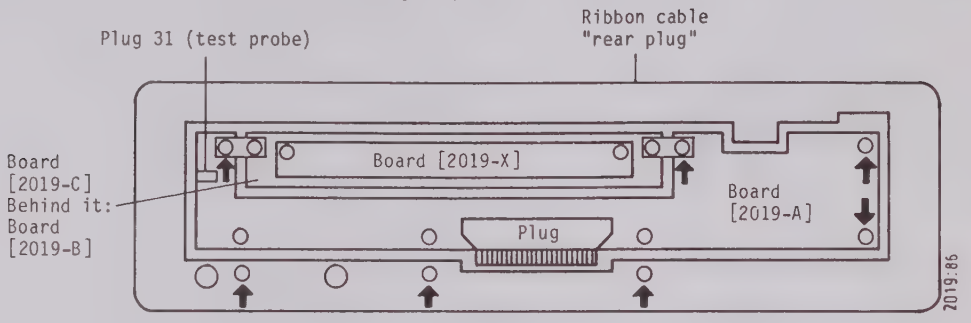


Fig. 3.3-4 Top view after removing the front panel

Detach connector 31 (test probe) and ribbon cable connector. After removing all Phillips screws (marked ⇧), the complete front unit can be lifted out from the front. The front unit is rendered functional by an extension ribbon cable* to board [2019-B] "Display control".

Luminous field [2019-X] (dismantling, replacement)

Remove the front panel.

Board [2019-X] is secured with 2 screws and additionally with double-sided adhesive tape on the display tube.

The ribbon cables are connected to board [2019-B] "Display control".

CAUTION: Dismantling of board [2019-X] "Luminous field" always causes destruction.

Note: When ordering a new board [2019-X], also order double-sided adhesive tape.

Front panel glass (dismantling, replacement)

Push the retaining clips out to the left and right (see Fig. 3.2-3).

Ordering information: Glass, PJM-4
Subject No. 2019-0000.026

* Test equipment No. 34-2019/2019-6500.012

3.3.2.4 "RF block" chassis

For troubleshooting on the "RF block"

Remove the "RF block" fastening screw (see Figs. 3.2-1 and 3.2-3).
Swing the "RF block" chassis up until it engages.

CAUTION: The chassis is not secured when swung up --> Risk of injury!

For troubleshooting on the "RF control"

Remove the fastening screws on the hinged "RF block" chassis (2 screws); also see Figs. 3.2-2 and 3.2-4.

"RF block" (dismantling)

Detach the ribbon cable on the RF control [2019-F], Subminax cable 2 St 3 (see Fig. 3.2-4), earthing cable on the "RF block" and the "RF block" Subminax connections (see Fig. 3.2-1). After removing the two screws marked A in Fig. 3.2-1, the entire "RF block" can be separated from the instrument.

3.3.2.5 (14) RF control [2019-F]

Dismantling

Swing up the "RF block".
Open the hinged "RF block" chassis (see Section 3.3.2.4, Paras. 1 and 2, and Fig. 3.2-4).
Detach the ribbon cable on the RF control [2019-F], the 16-pin ribbon cable on (14), wiring card [2019-E], and Subminax cable 14 St 1 on the RF control [2019-F].

Important: Remove (7) controller 2 [2019-N]. After removing all Phillips screws, lift the board slightly and slide carefully down and out of the chassis.

Assembly

Assembly is performed in the reverse order. When fitting (7) controller 2 [2019-N], ensure that the plug to the RF control is not alongside the socket.

3.4 INSTALLING OPTIONS

The PJM-4 can be retrofitted with the following options:

- Code error card (2) (4B3T, 5B6B, ECL 5B6B)
- Additional bit rates (4 freely-selectable bit rates)

The options can be installed at the factory or a service agency.
If the options are retrofitted at a service agency, refer to Sections 3.4.1 and/or 3.4.2.

3.4.1 <OPTION> (4) CODE ERROR CARD 2 (2019/00.01)

Currently only possible at the factory.

3.4.2 <OPTION> ADDITIONAL BIT RATES (2019/00.11)

The service agency itself can install the option from Series B onwards. It must first be established whether the service agency can perform calibration in accordance with Sections 8.5.1 and 8.6.1.

Ordering: The service agency completes Form 1

① Serial No.
② Instrument version
③ Existing options* (if any)
④ Device version*
⑤ Additional bit rates required

and sends it to:

Wandel & Goltermann GmbH & Co
Abt. Disposition
Postfach 1262
D-7412 Eningen u.A.

Note: The option supplied includes: - The necessary crystals for the bit rates
- The necessary potentiometers
- 1 EPROM

Depending on the additional bit rates required, the necessary crystals may have to be produced specially. This may result in a slightly longer delivery period.

* These entries are very important for programming the option EPROM.

PJM-4 Bit rate extension

INSTRUMENT DATA

FORM 1

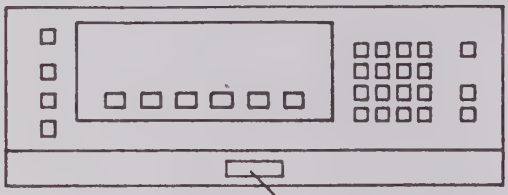
Bv. No.

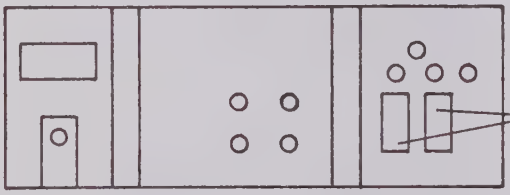
AB. No.

Order number 2019/00.11

Please complete the framed boxes only.

① Serial No. of instrument
② Instrument version
③ Existing options
④ Device version
⑤ Required bit rates
⑥ Company stamp, date, signature





Serial No.

①

②

PJM-4 Version	
BN 2019/01	
BN 2019/02	
BN 2019/03	
BN 2019/04	

PJM-4 Option	
BN 2019/00.01	
BN 2019/00.04	
BN 2019/00.10	
BN 985/21	

Called up via menu/as described*

③

_ _ _ _/_ _._ _

Options: _ _ _ _/_ _._ _._ _

Called up via menu/as described*

④

Device Version: 2019/_ _

* If not possible, state the complete signature No. of 90 IC 65 on CPU-2A.

⑤

Additional bit rates required

1.) _____ kbit/s
2.) _____ kbit/s
3.) _____ kbit/s
4.) _____ kbit/s
(5.) _____ kbit/s)

Please also enter additional bit rates already present. If existing additional bit rates are to be omitted or replaced by different ones, please make a clear note to this effect.

⑥ Company stamp Date Signature

Installation: - EPROM 90 IC 65, slot 7 on CPU-2A is replaced by the OPTION EPROM. The CPU card is accessible after removing the rear cover plate.
- After removing the housing base, the lock-in oscillator is accessible (see Fig. 3.2-2). The crystals are assigned to slots Q 106 ... Q 109 in ascending order to value. Refer to the component drawing and circuit diagram (6) "Carrier generation".

Alignment: As per Section 7.2.1.3.2

Calibration: As per Sections 8.5.1 and 8.6.1, as appropriate

Note: The OPTION EPROM is matched to the crystals fitted in the lock-in oscillator. Together, they form a single unit.

3.5 MAINTENANCE WORK

3.5.1 STORAGE BATTERIES (SERIES A, SERIES B...)

To replace the storage batteries, remove the lower housing cover. The storage batteries are to be found

in Series A: on the power supply unit (see Fig. 3.2-5)

in Series B...: alongside the power supply unit in the front housing section (see Fig. 3.2-2)

and can be replaced after removing the retaining bracket. Assembly is performed in the reverse order.

3.6 CLEANING WORK

Front panel and housing must not be cleaned with solvents:

- Solvents (e.g. naphtha or methylated spirit) may dissolve the lettering and impair the sharpness of its contours.
- Cleaners for plastic surfaces and furniture often have a polishing effect. They may damage the lettering and leave shiny marks on the cover plate.

The simplest cleaning liquid is warm water with a little added washing-up liquid. The cloth wetted with this water must only be damp. On no account must water be allowed to drip into the instrument. In order to avoid stripes and spots, the instrument should be wiped off with a dry cloth while still damp.

The CRT cover should only be cleaned damp, in order to avoid scratches and static charges.

Trifluoro-trichloroethane (TTE) can also be recommended for cleaning. TTE is non-inflammable, virtually non-toxic and odourless. It is an excellent solvent for all greases and oils, but does not attack paints and plastics. It is available under the tradenames Freon, Kaltron, Frigen and Flugène.

4 TROUBLESHOOTING: LOCALIZATION TO FAULTY ASSEMBLY 4-1

4.1 General notes on troubleshooting 4-1
4.2 Self-test for fault localization 4-1
4.2.1 Troubleshooting diagram for the instrument self-test 4-3
4.2.2 List of instrument error messages 4-4
4.2.3 List of other error messages and alarms for hardware faults 4-5
4.3 Service programs 4-5
4.3.1 Repair programs 4-5
4.3.2 Software test menus 4-6
4.4 Monitor programs (woris functions) 4-6
4.4.1 Operation with the instrument's own keyboard 4-6
4.4.2 Operation of the PJM-4 with the MONEX 4-6
4.5 Troubleshooting in the measuring section 4-7
4.5.1 General notes on troubleshooting in the measuring sections 4-7
4.5.2 Instrument fails to lock in ("SYNC LOSS" display) 4-8
4.5.2.1 Fault localization 4-8
4.5.2.2 Failure to lock in with jitter-free input signal 4-10
4.5.2.3 Failure to lock in with jittered input signal 4-14
4.5.3 Basic noise (inherent jitter) too high 4-18
4.5.3.1 General notes 4-18
4.5.3.2 Fault localization 4-19
4.5.3.3 Troubleshooting diagram 4-24
4.6 Possibilities for swapping circuits and/or functional groups 4-28
4.6.1 Swapping functional groups 4-28
4.7 Special test setups 4-31
4.7.1 Inherent jitter measurement, 11 MHz circuit 4-31
4.7.1.1 Inherent jitter measurement, controlled 11 MHz circuit 4-33
4.7.1.2 Inherent jitter measurement, 11 MHz circuit, with uncontrolled 11 MHz VCO 4-34
4.7.2 Inherent jitter measurement, 220 MHz circuit 4-34
4.7.3 Testing the control limit frequency of the 220 MHz circuit 4-39
4.8 Circuit-related block circuit diagram 4-41
4.9 Booting 4-41

4 TROUBLESHOOTING: LOCALIZATION TO FAULTY ASSEMBLY

4.1 GENERAL NOTES ON TROUBLESHOOTING

Troubleshooting best starts by considering whether the fault is to be found in the digital section or the measuring section. The instrument includes a self-test feature for the digital section (see Section 4.2) to facilitate this decision.

A fault in the digital section certainly exists if the test in Section 4.2.1 does not run in the manner described.

There is no self-test feature for checking the measuring section. It must be checked in accordance with Section 4.5.

Faults in transmission from the digital section to the measuring section and vice versa can be defined more accurately by using the tests in Section 4.5 (Troubleshooting in the measuring section). The service programs as per Section 4.3 and the monitor programs as per Section 4.4 are also available for this purpose.

! Important note !

It is best to replace faulty circuits and functional groups (see Section 4.6).

4.2 SELF-TEST FOR FAULT LOCALIZATION

General notes on the self-test

A self-test program is executed automatically when the instrument is switched on.
The following tests are executed in the order given:

Function tested	Test result
Display test	
Key LEDs	All ON
Luminous field LEDs	All ON
Display	Alternately, every 2nd display point and every 2nd cursor position ON
CPU test	
	The following applies for all subsequent tests:
RAM	If a fault is detected, it is indi-
ROM	cated as follows (Section 4.2.2):
I/O	1. Error No. in display
	2. Key LED identification
	3. Tone sequence
IEC bus	
Keyboard	If no fault is detected:
Clock module	Display as per stored instrument setup or as per basic settings

Further procedure if a fault is detected:

CPU fault : Instrument displays fault and performs no further actions.
All other faults: Instrument operable at end of test - press RETURN key to continue.

Separate call for the self-test program:

A self-test program (Section 9.3.1) can be called up via the software test menu (Section 9.3). Refer to Section 9.3.3 for a description.

Note on the "Clock module" test (error 1003):

If the power supply unit has been replaced, the time is lost. Consequently, the instrument reports a self-test error when switched on again, since a meaningless date is loaded.

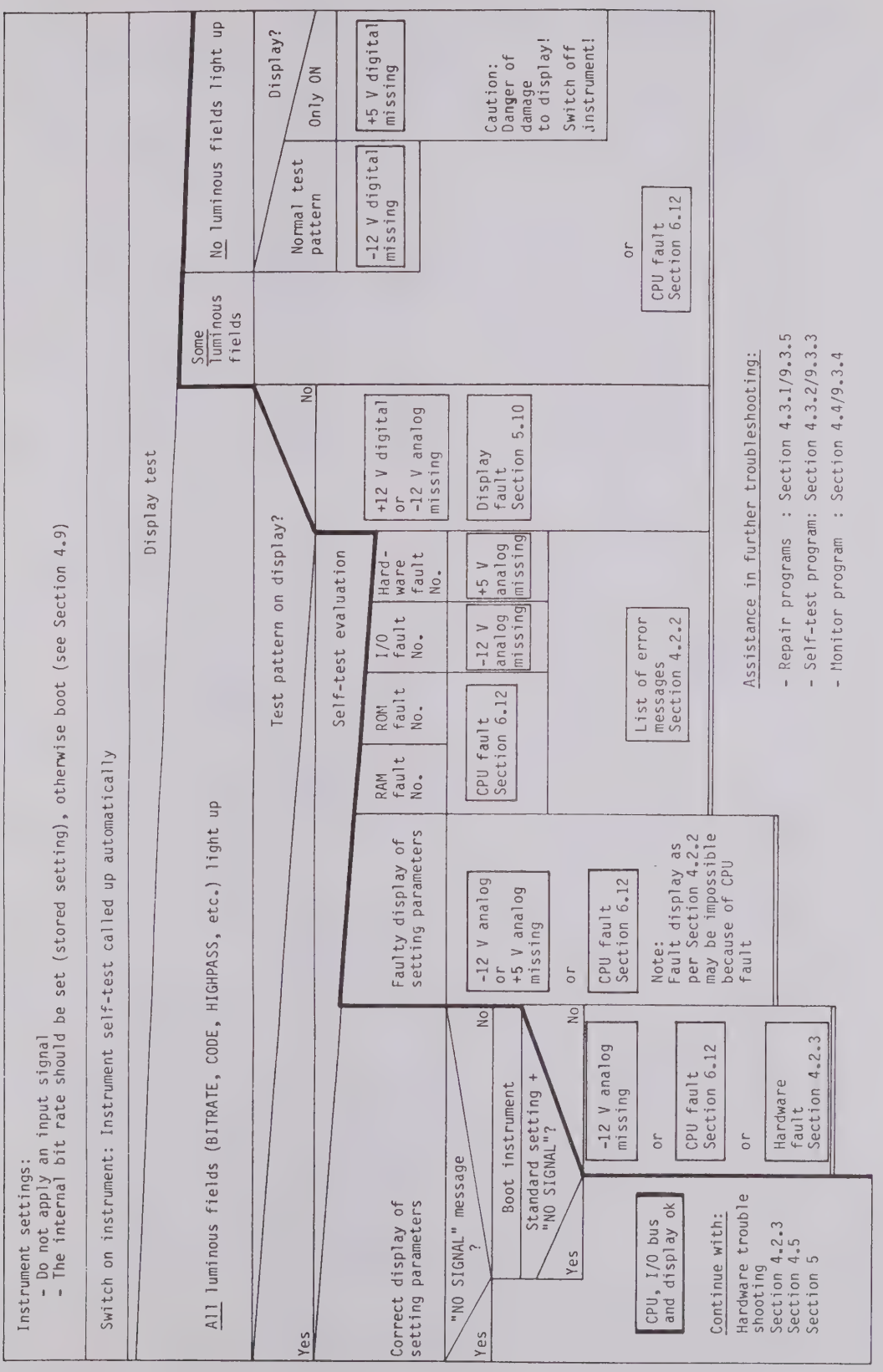
If time and date can be set again, this error message can be ignored.

Note: If this error message appears although the power supply unit has not been replaced, and if the time can be set again, this indicates a failure of the back-up batteries.

Note on troubleshooting:

Whenever instrument error messages occur, always check the operating voltages before any further troubleshooting!
Refer to the information in the troubleshooting diagram in Section 4.2.1.

4.2.1 TROUBLESHOOTING DIAGRAM FOR THE INSTRUMENT SELF-TEST



4.2.2 LIST OF INSTRUMENT ERROR MESSAGES

Error No. on display	Dark LED	Tone sequence 2 x	Fault	Fault location
		CPU TEST		
			Wrong EPROM checksum	
100	"LEAD"	HLL	ROM 00 90IC61	
101	"LEAD"	HLL	ROM 01 90IC62	
102	"LEAD"	HLL	ROM 02 90IC63	
104	"LEAD"	HLL	ROM 04 90IC65	=> CPU
			RAM fault	
200	"TRAIL"	LLL	RAM 0 90IC66	
201	"TRAIL"	LLL	RAM 1 90IC67	
202	"TRAIL"	LLL	RAM 2 90IC68	
203	"TRAIL"	LLL	RAM 3 90IC69	=> CPU
		I/O BUS TEST		
300	"$\sqrt{f}$ "	LLH	I/O bus fault	=> CPU => Other cards
		DISPLAY TEST		
511	- -		Data transmitted to the display control are not allowed for the currently valid command	=> CPU => I/O bus
512	- -		Master computer transmits an unknown command	=> CPU => I/O bus
		IEC BUS TEST		
600	"DATA"	HHH	IEC bus fault (Not checked at Mains ON)	=> IEC bus card
		HARDWARE TEST		
1001	"PANEL LOCK"	LHL	No 10 Hz clock	=> Peak rectifier
1002	"PANEL LOCK"	LHL	Key pressed during test	=> Keyboard
1003	"PANEL LOCK"	LHL	Time lost	=> Hit counter
1004	"PANEL LOCK"	LHL	Clock module blocked	=> Hit counter
1005	"PANEL LOCK"	LHL	CPU DIP switch not in defined position (test continues after display)	=> CPU

Also refer to the notes overleaf.

Notes:

Errors 100 ... 600 : Error display not guaranteed; instrument perfoms no further actions

Errors 1001 ... 1004: Instrument operable at end of test

Error 1003 : Observe note in Section "General notes on the self-test" without fail!

When troubleshooting: Observe corresponding note in Section "General notes on the self-test" without fail.

4.2.3 LIST OF OTHER ERROR MESSAGES AND ALARMS FOR HARDWARE FAULTS

Only the error messages important for hardware troubleshooting are listed here.
See Section 3.5.2 of the Operating Instructions for a complete list.

1. "INPUT OVERLOAD"
   If no input signal is applied, or if it is known to have normal amplitude, the following faults are possible:

   a) Operating voltages missing -12 V analog => Section 5.11
   -5.2 V (generated on RF control)

   b) Input circuit faulty => Section 5.2

2. "NO SIGNAL"
   If an input signal is applied, the following faults are possible:

   a) Operating voltage missing +12 V analog => Section 5.11
   b) Input circuit faulty => Section 5.2
   c) RF control faulty => Section 5.7

3. "SYNC LOSS"
   Correct input signal applied, PJM-4 set to correct bit rate:

   a) Operating voltage missing +12 V analog => Section 5.11
   b) Fault in RF block, PLL circuits cannot lock in => Section 4.5.2

   If no input signal applied:

   a) Operating voltage missing -6.2 V => Section 5.11
   b) Fault in input section => Section 5.2

4.3 SERVICE PROGRAMS

4.3.1 REPAIR PROGRAMS

The following programs are available for hardware troubleshooting:

- Address decoder test: A0H ... ABH, B0H ... BFH } RF control (14)
  80H ... 97H Hit counter (13)
  C0H ... E6H Filter (11), Rectifier (12), Code error 1 (3)
- DAC test for : Current source, sawtooth meter (7)
  Lock-in DAC, Equalizer DAC } RF control (14)
  Hit counter threshold DAC (13)

- LED test
- Luminous field test
- Keyboard test
- Display test

Use: For troubleshooting on assemblies (Section 5) and circuit boards (Section 6)

Description and calling up: See Section 9.3.5

4.3.2 SOFTWARE TEST MENUS

A number of further utility programs based on a menu system are available for testing and service purposes:

- Various self-test program versions without normal instrument functions
  Use: For fault localization, see Section 4.2
- "ENTW" test menu: Allows intervention in instrument control with otherwise normal instrument functions.
  Use: Mainly for troubleshooting in the measuring section, see Section 4.5

Description and calling up: See Sections 9.3 to 9.3.3

4.4 MONITOR PROGRAMS (WORIS FUNCTIONS)

4.4.1 OPERATION WITH THE INSTRUMENT'S OWN KEYBOARD

The integrated "SERVICE" monitor software is called up via the utility program menu.
All WORIS functions are available.
In this context, refer to:

Section 9.3	Calling up the menu
Section 9.3.1	Menu table
Section 9.3.4	Instrument key assignments for "SERVICE"

The monitor program can only be exited by:
a) Instrument OFF/ON
b) S:0000

4.4.2 OPERATION OF THE PJM-4 WITH THE MONEX

The software for operation with the external MONEX control section is integrated into the PJM-4.

- See Section 2.3.3 for a description
- See Section 2.3.4 for adaptation and notes on the use of the external MONEX

4.5 TROUBLESHOOTING IN THE MEASURING SECTION

4.5.1 GENERAL NOTES ON TROUBLESHOOTING IN THE MEASURING SECTIONS

The measuring section (all assemblies except power supply unit and display/control section) can be divided into two parts:

a) The evaluation circuit with : - Filter card
- Rectifier card
- Code error card

b) The hinge-mounted RF chassis with : - Frequency generator
- Input section
- 220 and 11 MHz circuit
- Adder
- RF control

See Section 5 for troubleshooting in the evaluation circuit.

Troubleshooting in the RF section is far more complicated, particularly in the event of faults in the PLL circuits.

This Section contains instructions on systematic troubleshooting for two typical faults:
- The instrument fails to lock in
- Excessive intrinsic jitter display.

Notes on troubleshooting:

1. The specified method for troubleshooting (fault localization, troubleshooting diagram) should be observed!
   As the PLL circuits are coupled, there is a risk of erroneous conclusions when assigning fault causes during troubleshooting unless certain secondary conditions are observed during troubleshooting.
   A repair attempted unnecessarily may entail considerable alignment work throughout the instrument.
2. Alignments should only be changed once the cause of the fault has been established conclusively - never in order to find the cause of a fault!
   Above all, the alignments of the phase meters (11 MHz phase meter, sawtooth phase meter) should never be changed without good reason. The 11 MHz phase meter can only be aligned correctly in the factory.
3. When troubleshooting, it may be helpful to swap circuits by way of experiment. Section 4.6.2 provides information as to the effects on the instrument functions if a necessary alignment is not performed after swapping circuits. If the resultant limitation of the instrument function is irrelevant for troubleshooting, the troubleshooting work should be continued without this alignment (the alignment is made when the repair is completed) or the circuits returned to their original positions.

4.5.2 INSTRUMENT FAILS TO LOCK IN ("SYNC LOSS" DISPLAY)

4.5.2.1 Fault localization

The following questions must be checked:

1. Correct instrument setting? (See Operating Instructions)
   - Bit rate frequency?
   - Clock/Data setting?
   - Code setting?
   - Measuring range exceeded?
2. Input signal correct?
   - If the expected jitter is within the measuring range limits
     => Try again with a second PJM-4 or good generator signal.

If no cause of the fault can be found in this way, an instrument fault must be assumed.

A jitter-free clock signal source at least is required for further troubleshooting; a PJG-4 is even better.

Troubleshooting diagram for rough fault localization:

<table>
<tr><td colspan="5">Apply a jitter-free input signal</td></tr>
<tr><td colspan="3">Instrument locks in?</td><td colspan="2" rowspan="2"></td></tr>
<tr><td>No locking-in at <u>one</u> bit rate</td><td>No locking-in at <u>all</u> bit rates</td><td><u>Always locks in</u></td></tr>
<tr><td>See Note a)</td><td>See Note b)</td><td colspan="3">Jitter input signal.
Vary jitter amplitude and frequency, but always within the permissible measuring range limits for the set bit rate
(see Section 1.4.1.3 of Op. Instr.)</td></tr>
<tr><td rowspan="3">Troubleshooting: Section 4.5.2.2</td><td rowspan="3"></td><td colspan="3">Instrument locks in within measuring range limits?</td></tr>
<tr><td>No locking-in at one bit rate</td><td>No locking-in at all bit rates</td><td>Always locks in</td></tr>
<tr><td>See Note d)</td><td>See Note c)</td><td>PJM-4 ok</td></tr>
<tr><td colspan="2">Troubleshooting: Section 4.5.2.3</td><td>Measuring error</td></tr>
</table>

Notes on the troubleshooting diagram:

Re a): Troubleshooting in the PLL circuits: => Section 4.5.2.2
or first check the following circuits:

1. Frequency generator:

   Check the frequency of the regenerated clock
   Suspicion: Frequency generator not supplying a signal (lock-in oscillator);
   therefore, regenerated clock frequency = 0
   => Section 5.1
   => Section 9.3.1 (Test menus for measuring/displaying f_{reg})

2. Saw-tooth phase meter:
   Check sawtooth oscillation (wave form)
   Suspicion: Wrong charging current for sawtooth phase meter due to hardware fault
   => Section 6.7

Re b): Troubleshooting in the PLL circuits: => Section 4.5.2.2

Re c): Troubleshooting in the PLL circuits: => Section 4.5.2.3
or first check the following circuits:

1. 11 MHz phase meter:
   Suspicion: U_{ref} wrong
   => Section 6.9

2. Controller 1:
   Suspicion: Fast/slow switching
   => Section 6.11

3. Sawtooth phase meter:
   Suspicion: U_{ref} wrong
   => Section 6.7

4. Continue with d)

Re d): Troubleshooting in the PLL circuits: => Section 4.5.2.3
or first check the following circuits:

1. 220 MHz circuit:
   Check control limit frequency => Section 4.7.4
   Suspicion: - Controller 2 : Incorrect gain (input divider)
   => Section 6.6
   - 220 MHz VCO : Change in slope
   => Section 6.5

2. Sawtooth phase meter:
   Check sawtooth oscillation (wave form)
   Suspicion: Incorrect charging current for sawtooth phase meter due to hardware fault
   => Section 6.7

4.5.2.2 Failure to lock in with jitter-free input signal

Precondition:

Successful instrument self-test (Section 4.2)

The notes in Section 4.5.2.1 on fault localization and excluding measuring errors should also be observed!

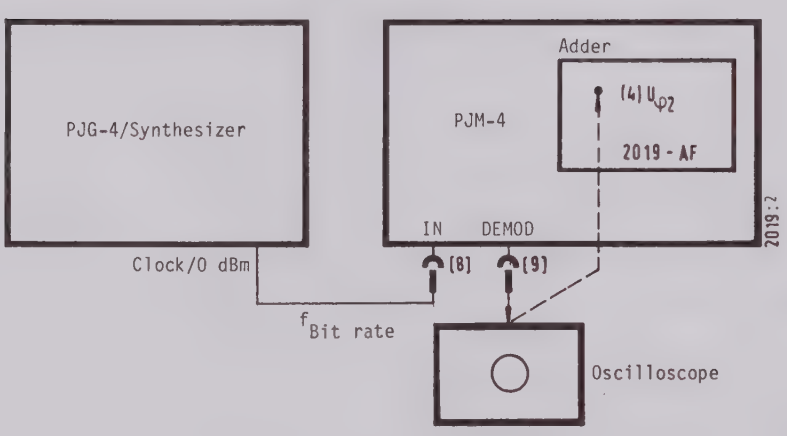
Instruments required:

1 PJG-4 (or other jitter-free signal source capable of supplying the bit rate frequency, e.g. synthesizer)
1 oscilloscope BW > 20 MHz

Software aids used:

"ENTW" test menu: Calling-up : Sections 9.3 and 9.3.1
Description : Section 9.3.2

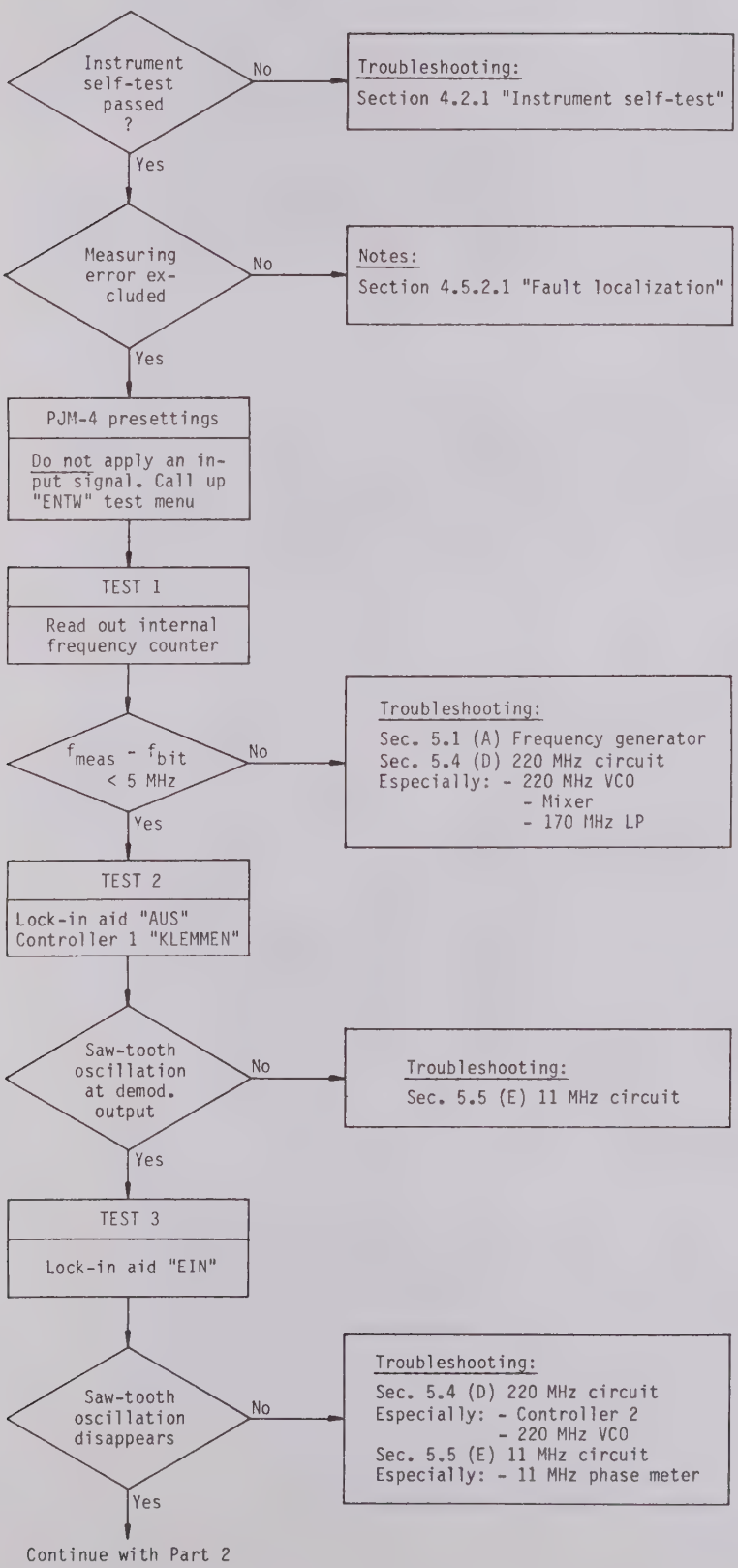
Test setup:



List of tests to be performed:

TEST 1 : Frequency generator
TEST 2 ... 4: Lock-in aid function
TEST 5 ... 6: 220 MHz circuit
TEST 7 : Automatic lock-in procedure
TEST 8 ... 9: 11 MHz circuit lock-in procedure

Troubleshooting diagram to
Section 4.5.2.2 (Part 1)



4.5.2.3 Failure to lock in with jittered input signal

Precondition:

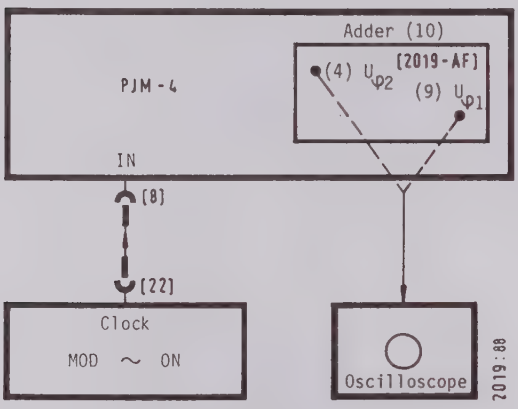
The instrument locks in with a jitter-free input signal and the troubleshooting diagram to Section 4.5.2.2 was completed without faults.

The following troubleshooting diagram is the continuation of Section 4.5.2.2.

Required instruments and software aids:

See Section 4.5.2.2

Test setup:

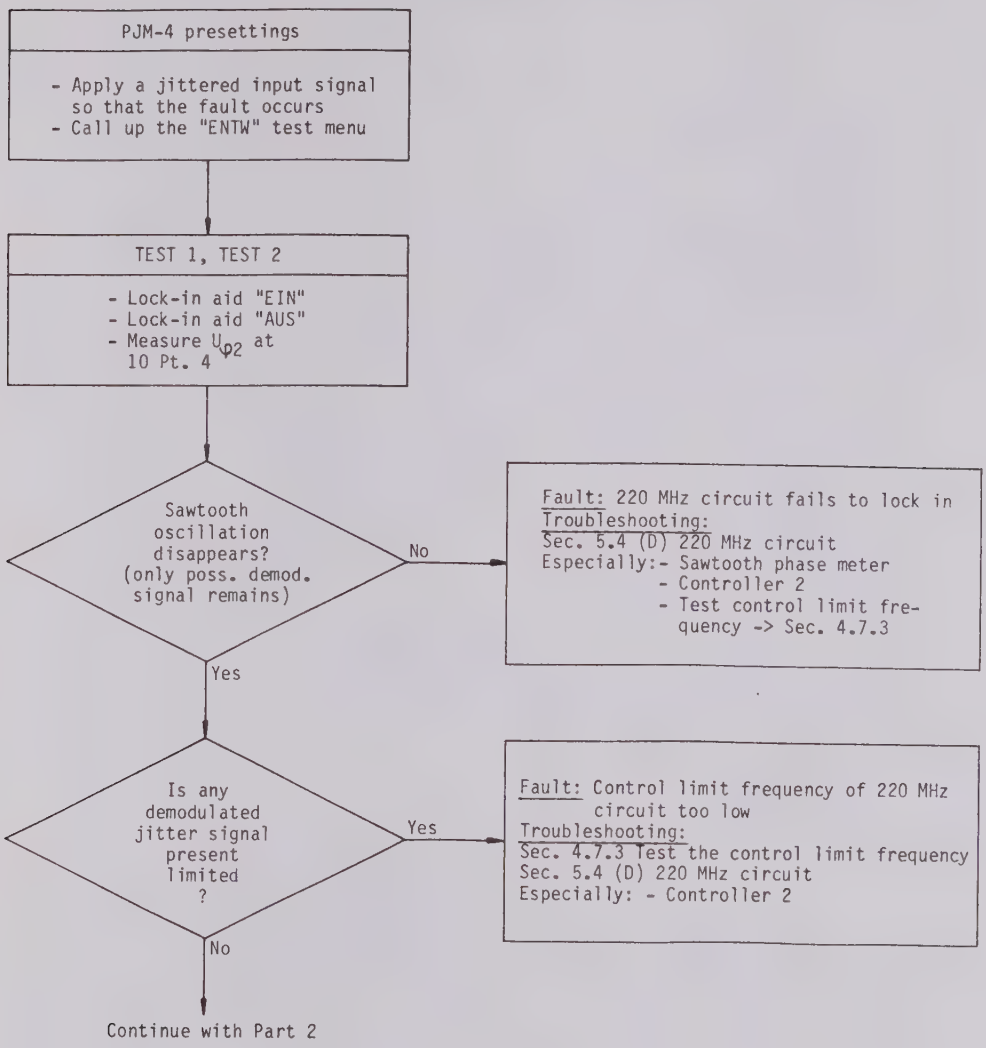


List of tests to be performed:

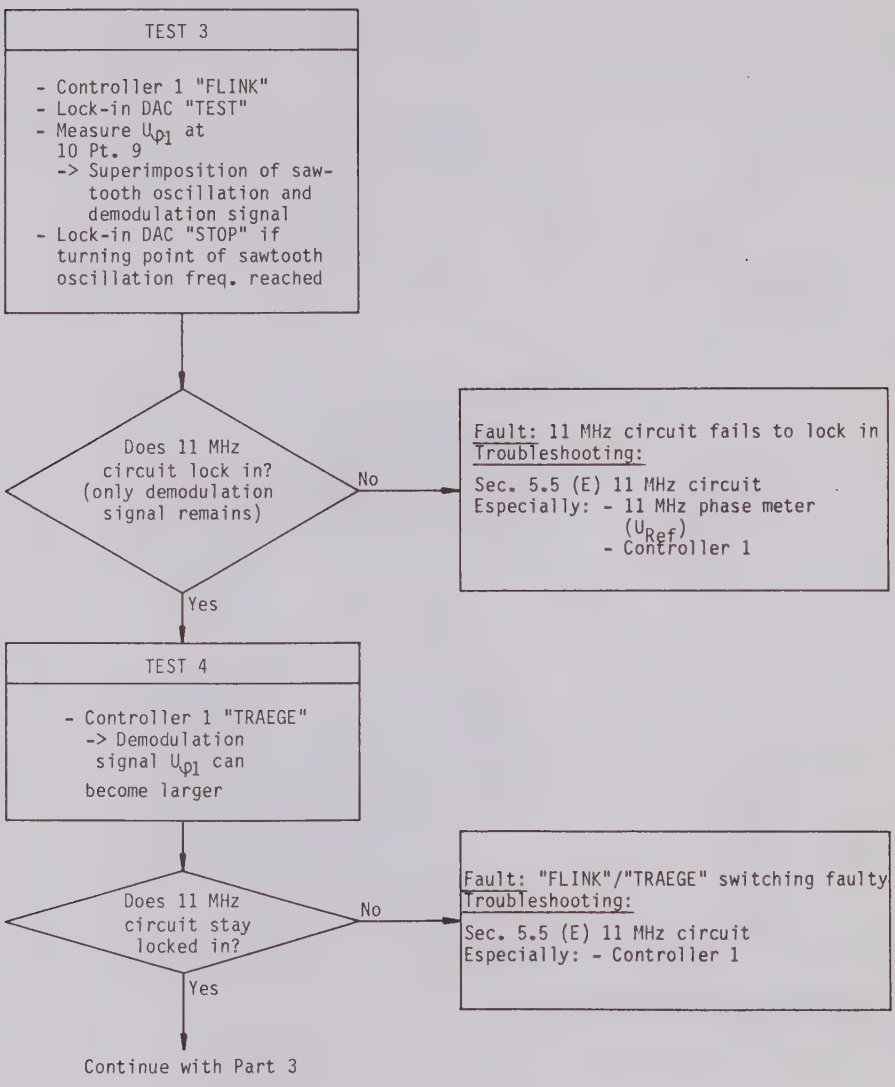
TEST 1: Does the 220 MHz circuit lock in?
TEST 2: Is the 220 MHz circuit overloaded?
TEST 3: Does the 11 MHz circuit lock in after stopping the search manually?
TEST 4: Does the 11 MHz circuit remain locked in after manual "FAST"/"SLOW"* switching?
TEST 5: Does the automatic "FAST"/"SLOW"* switching function work?

* "FLINK"/"TRAEGE"

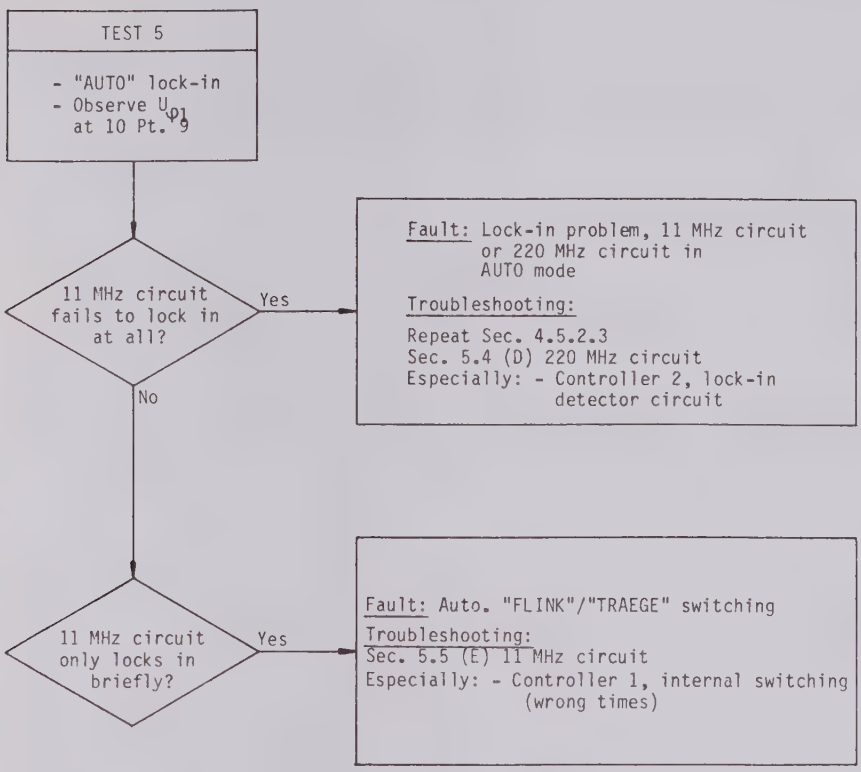
Troubleshooting diagram to Section 4.5.2.3 (Part 1):



Troubleshooting diagram to Section 4.5.2.3 (Part 2):



Troubleshooting diagram to Section 4.5.2.3 (Part 3):



4.5.3 BASIC NOISE (INHERENT JITTER) TOO HIGH

4.5.3.1 General notes

If excessive inherent jitter is suspected, first check the quality of the signal source, e.g. by performing a comparison with another PJM-4 or a different signal source.

Call up testprogram BASIC NOISE!

1. Switch off the instrument.
2. Hold down the 2 key (on the front panel).
3. Switch on the instrument and hold down the 2 key until a short BEEP is heard (ignore hardware ERROR 1002).
   Measured with clock signal, possibly from a good synthesizer (e.g. Racal Dana)

Bit rate [kbit/s]	HP [Hz]	LP [kHz]	Limit test value [mUI_{pp},AV]	Typ. [mUI_{pp},AV]
2048	2	185	7	6
8448	2	600	8	7
25776	2	600	8	7
< 30000	2	600	8	7
34368	2	1200	20	8
139264	2	6700	20	17
> 30000	2	6700	20	17

Data signal, 2E23-1 sequence, from PJG-4, modulation EXTERNAL and open, CMI code:

139264	2	6700	35	30

(Note: Test the inherent PJG-4 jitter with a good PJM-4)

Fig. 4.5-1 Table: Measured values for basic noise

Relationship between inherent jitter and clock/data signal:

At low bit rate frequencies (< 34 Mbit/s), there is usually no detectable major increase in the inherent jitter with data signals.

Here, therefore, the "excessive inherent jitter" fault usually occurs with both clock and data signals.

Result: In "normal" circumstances, troubleshooting can be carried out with a clock signal of good spectral purity, meaning that no inherent jitter components of a data signal generator need be taken into account.

Exception: E.g. excessive intrinsic jitter at 139 Mbit/s and CMI code.

Important notes on troubleshooting/measuring technique:

1. Special test setups are specified for testing the inherent jitter of the 220 MHz circuit, input circuit and 11 MHz circuit (Section 4.7). Unambiguous testing during normal operation is not possible.
   Reason: The signals of both circuits are added in the adder. Interruption of the one signal path does not produce solely the inherent jitter component of the other.

220 MHz circuit: Jitter suppression below the control limit frequency; interference of the 220 MHz VCO is also measured at higher values (emphasized when added).

11 MHz circuit : In normal mode, the output signal contains all (possibly overemphasized) interferences of the frequency generator.

2. No direct measurement of the frequency generator is provided for (highly complicated). Therefore, it is tested indirectly by excluding other fault causes.

Troubleshooting sequence:

1. Localize the fault:
   Determine the type of fault, if possible
   See Section 4.5.3.2, Table 4.5-5, for notes
2. Establish the faulty functional group as per the troubleshooting diagram in Section 4.5.3.3
3. Localize to the faulty circuit:
   a) See section 4.5.3.2, Table 4.5-6, for notes
   b) See Section 5 for further information on troubleshooting in the functional group concerned.

4.5.3.2 Fault localization

The type of inherent noise should be determined in order to localize the fault. The filter functions built into the PJM-4 can be used for this purpose. An analyzer can be connected to the DEMOD output for further spectral analysis.

Check the operating voltages for interference prior to any further troubleshooting.

Notes on working with the analyzer (SNA-1):

Connect the SNA-1 to [9] DEMOD output, PJM-4

- High-frequency interference:

  e.g. Bit rate : 25 Mbit/s, clock
  Generator : Synthesizer (poss. PJG-4)
  PJM-4 bandwidth : 100 Hz - 1200 kHz
  SNA-1 : REFERENCE = -50 dB, SCALE = 100 dB, AVRG
  FSTART = 100 kHz, FSTOP = 1 MHz
  RBW = 1 kHz

  Lines:
  A line with -86 dB, for example, produces a noise of 1 mUI

  Noise (mid-band) ..... < -115 dB

  See Figs. 4.5-2 and 4.5-3

  Digital reading
  Call up testprogram BASIC NOISE (see section 4.5.3.1)
  100 Hz - 1200 kHz ..... < 5 mUI
  100 Hz - 600 kHz ..... < 4 mUI

- Search for mains hum:

  PJM-4 bandwidth : 2 Hz - 600 kHz
  SNA-1 : FSTART = 0 Hz, FSTOP = 1 kHz
  RBW = 10 Hz

  Hum lines ..... < -90 dB

  See Fig. 4.5-4

Permissible operating voltage interference (measured on RF chassis):

Referred to all voltages < 10 mV_{pp}, lines: < -50 dB

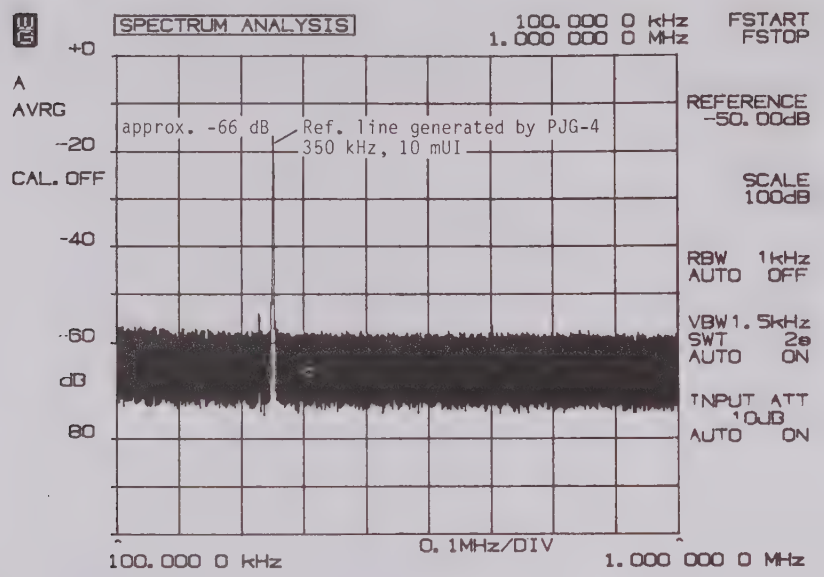


Fig. 4.5-2 Basic noise, mid-band with reference line

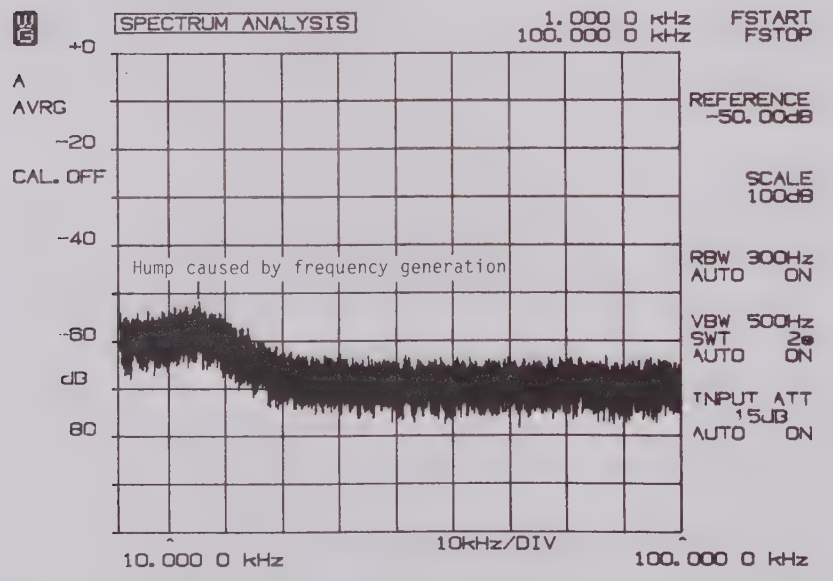


Fig. 4.5-3 Noise magnitude, frequency generator

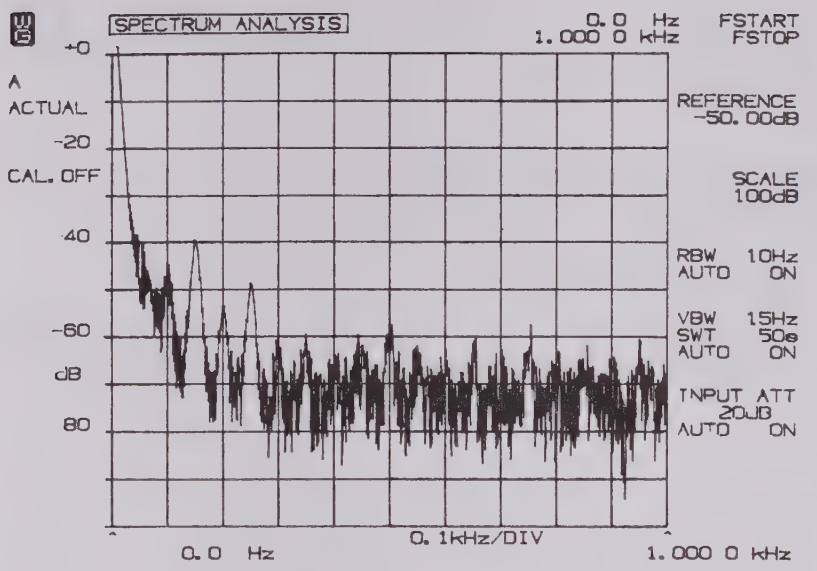


Fig. 4.5-4 Hum lines

Fault localization table:

This Table shows possible ways of differentiating between types of jitter interference and gives pointers as to the (typical) cause of the fault or the possible fault location.

Call up testprogram BASIC NOISE (see section 4.5.3.1)

Signal type	Type of jitter interference	Possibility for differentiation	Possible fault cause/location
CLOCK SIGNALS	Low-frequency interference	Raise HP level: Displayed inherent jitter decreases: e.g. jitter ok for HP > 10 Hz	Interference from crystal oscillators: a) Frequency generator: Lock-in oscillator b) 11 MHz circuit: 11 MHz VCO Intermittent fault (phase hits): 11 MHz circuit: e.g. feed-through Cs Addition error: Adder: 220 MHz path interrupted
	Interference lines	Connect analyser to demod. output: Generate Ref. level with PJG-4 and 10 mUI span in order to assess interference line effect	Approx. 200/400 kHz: Power supply unit interference: a) Possibly filtering in one circuit of the RF circuit faulty b) Power supply unit interference too great c) Filter/rectifier card: Faulty filtering Other lines, particularly if bit rate-dependent: a) Frequency generator b) 220 MHz circuit: Mixer 220 MHz VCO
	Noise	Assess by reducing bandwidth or by connecting analyzer to demod. output	Wideband noise level: 11 MHz circuit: 11 MHz phase meter Noise increase (to approx. 10 kHz) Frequency generator: Carrier phase meter

Fig. 4.5-5 Fault localization table - Part 1

Signal type	Type of jitter interference	Possibility for differentiation	Possible fault cause/location
D A T A S I G N A L S	Usually wideband interference	Determine bit rate/ code combination at which inherent jitter too high	Fault only with 139 Mbit/CMI: a) Input circuit b) 220 MHz circuit: Saw-tooth phase meter Fault only with certain codes and/or edges (where allowed): Input circuit

Fig. 4.5-5 Fault localization table - Part 2

Table of all circuits contributing towards the inherent noise:

(higher in the event of a fault)

Functional group	Faulty circuit	Inherent noise caused (typical)
Input section (B)	Input section	Jitter with data signal
220 MHz circuit (D)	Sawtooth phase meter Mixer	Jitter with data signal Interferance lines
11 MHz circuit (E)	11 MHz phase meter 11 MHz VCO Controller 1	Noise/low-freq. interference Low-frequency interference Low-frequency interference
Frequency generator (A)	Lock-in oscillator Carrier phase meter	Low-frequency interference Noise (PLL raised)
Adder (F)		Noise
Filter (H) and peak rectifier (K)		Noise (Sensitive to operating voltage interference)

Fig. 4.5-6 Table of circuits causing inherent noise

4.5.3.3 Troubleshooting diagram

Instruments required:

Synthesizer: High spectral purity, output level 0 dBm (better +6 dBm)
e.g. Racal Dana, R & S SMG

Frequencies required:
TEST 3 220 MHz
TEST 4 Bit rate frequency
TEST 5 Bit rate frequency +220 MHz

PJG-4 : For TEST 6 Troubleshooting with excessive inherent data signal jitter (check the inherent jitter of the PJG-4 with a good PJM-4)

Analyzer : SNA-1

Test list:

TEST 1: Filter/rectifier card
TEST 2: Adder
TEST 3: 11 MHz circuit See test setup in Section 4.7.1
TEST 4: 220 MHz circuit See test setup in Section 4.7.2
TEST 5: Frequency generator
TEST 6: Inherent jitter with data signals

Note the following:

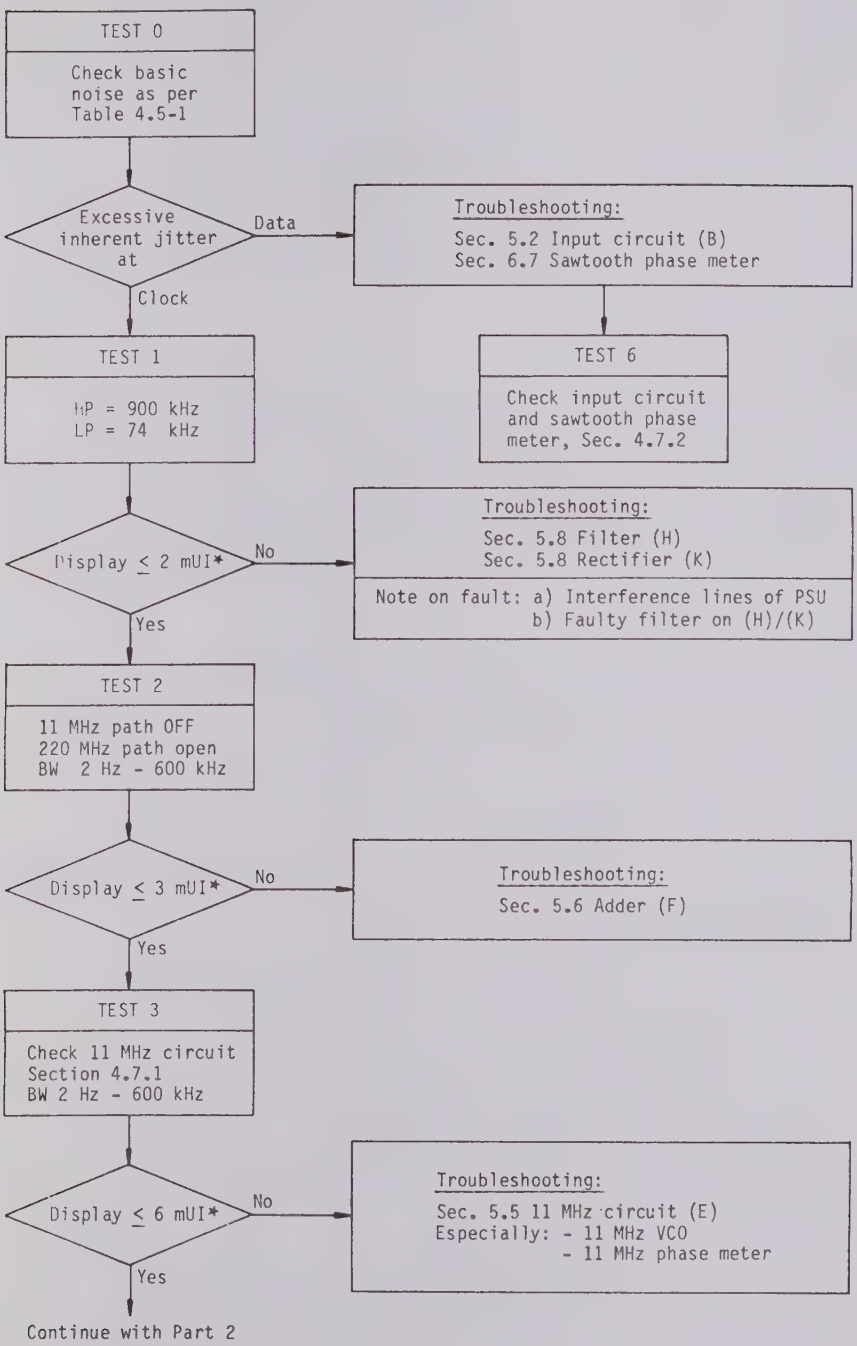
After every completed test, change the PJM-4 back again, unless the same changes are prescribed for the next test!

Prior to any troubleshooting in the measuring section:

Check the operating voltage interference. Refer to the notes in Section 4.5.3.2.

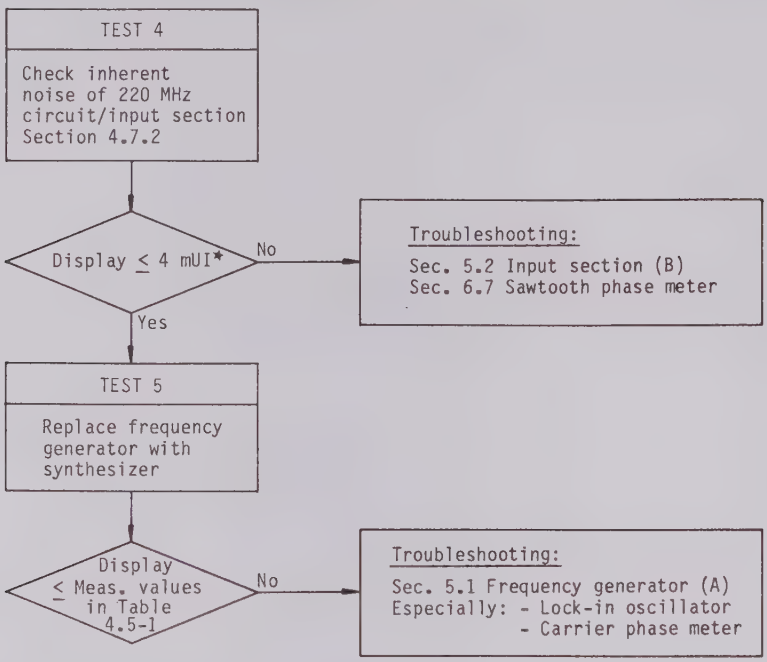
Troubleshooting diagram, Part 1:

Detailed TEST description at end of flow chart



* Call up testprogram BASIC NOISE (see section 4.5.3.1)

Troubleshooting diagram (Part 2):



TEST 1: Test filter/rectifier

- PJM-4 locked in, bit rate and generator on any setting
- Set overlapping HP/LP filters: HP = 900 kHz
  LP = 75 kHz
  (Flashing display normal)
- Digital value ..... $\leq$ 2 mUI_{pp}*

TEST 2: Test adder

- Operate PJM-4 without input signal
- In adder: 11 MHz path OFF : Flip 10 S 3
  220 MHz path OFF: Open 10 S 4 (note original switch setting)
- Set via "ENTW" test menu:
  In "EING-STUFE" menu: Input divider = 20 dB
  In "RAST-EINST" menu: Lock-in aid "EIN"
  Use RETURN key to return to measuring program

Digital value (2 Hz - 600 kHz) ..... $\leq$ 3 mUI_{pp}*

=> If fulfilled, adder ok, but 10 IC 10 not yet tested.

Test with 10 IC 10: - Remove controller 1
- Connect adder input 10 Pt. 9 to ground
- Use test menu to make same settings as above

Digital value (2 Hz - 600 kHz) ..... $\leq$ 3 mUI_{pp}*

* Call up testprogram BASIC NOISE (see section 4.5.3.1)

TEST 3: Test inherent noise of 11 MHz circuit

- Perform measurement as per Section 4.7.1

Digital value (2 Hz - 600 kHz) ..... $\leq$ 6 mUI_{pp}*

2 Hz - 74 kHz ..... $\leq$ 5 mUI_{pp}*

10 Hz - 74 kHz ..... $\leq$ 3 mUI_{pp}*

100 Hz - 600 kHz ..... $\leq$ 4 mUI_{pp}*

For 139 Mbit/s setting only:

2 Hz - 6700 kHz ..... $\leq$ 15 mUI_{pp}*

TEST 4: Test inherent noise of 220 MHz circuit/input circuit

- Perform measurement as per Section 4.7.2, Measurement 1

Digital value (2 Hz - 600 kHz) ..... $\leq$ 4 mUI_{pp}*

For 139 Mbit/s:

2 Hz - 6700 kHz ..... $\leq$ 4 mUI_{pp}*

Note: In this measurement, the basic noise of the evaluation circuit (adder, filter/ rectifier) typically determines the digital value.

TEST 5: Inherent noise of frequency generator

No direct measurement of the inherent noise due to complexity

- Instrument settings:

  PJM-4: - Remove carrier oscillator and apply 220 MHz + bit rate frequency with 0 dBm from synthesizer at 5 Pt. 16 (Ri approx. 50)

  - Set bit rate and corresponding bandwidth

- Bit rate clock signal from PJG-4 (better: 2nd synthesizer) at PJM-4 input

Digital value ..... < Corresponding measured value from Table 4.5-1

If a PJG-4 is used as bit rate generator, the jitter displayed may be slightly above the values in the Table, even without an instrument fault.

TEST 6: Inherent jitter for data signals*

- Perform measurement as per Section 4.7.2, Measurement 2

Digital values:

139 Mbit/s

10 Hz - 6700 kHz, CMI ..... < 30 mUI_{pp}*

NRZECL ..... < 25 mUI_{pp}*

34 Mbit/s

10 Hz - 1200 kHz, AMI ..... < XX mUI_{pp}*

25 Mbit/s

10 Hz - 600 kHz, AMI ..... < XX mUI_{pp}*

8 Mbit/s

10 Hz - 600 kHz, AMI ..... < XX mUI_{pp}*

---

* Call up testprogram BASIC NOISE (see section 4.5.3.1)

4.6 POSSIBILITIES FOR SWAPPING CIRCUITS AND/OR FUNCTIONAL GROUPS

4.6.1 SWAPPING FUNCTIONAL GROUPS

The following functional groups are suitable for complete swapping:

1. RF chassis and code error:

No further instrument alignment is required in this case. Consequently, this procedure is particularly suitable if there are no possibilities for alignment and the fault is clearly located in the area of the following functional groups:

- Frequency generator (A)
- Input circuit (B)
- 220 MHz circuit (D)
- 11 MHz circuit (E)
- Adder (F)
- RF control (G)
- Code error (C)

2. RF chassis without code error:

In this case, the code error card must be aligned after swapping.
If there are no possibilities for alignment, code error detection is usually still guaranteed, although the jitter tolerance may be considerably restricted.

3. Display/control section (L):

There are no restrictions on swapping the hardware and no alignment is required.
However, the software statuses in EPROM 16 IC 15 on the display control and on the master computer must match. This can be checked on the basis of the signature lists.

For further notes on swapping circuits, see:

- Section 4.6.2 Effect on instrument function and alignment of swapping individual circuits
- Section 7.1 List of alignments

4.6.2 EFFECTS OF SWAPPING INDIVIDUAL BOARDS

The Table below provides information on:

- The alignment conditions after swapping boards
- The consequences of inability to carry out alignment, e.g. when swapping between individual instruments during troubleshooting or if the instrument is not available for alignment.

Prerequisite: Tested and, where specified, aligned replacement boards.

Alignment instructions: See Section 7.1.2

Explanations to the Table: At the end of the Table (next page)

Circuit swapped	Align-ment	Other circuits to be aligned (instrument alignment)	Restrictions if alignment not performed
Freq. generator (A)			
Carrier oscillator	A	-	-
Carrier phase meter	GF	-	Inherent noise
Lock-in oscillator	A	-	-
Clock divider	-	-	-
Input circuit (B)	A	Code error	Jitter tolerance Code error detection
220 MHz circuit (D)			
220 MHz VCO	A	Controller 2	Measuring range for jitter spans > 0.5 UI_{ss}
Controller 2	GF	-	(see Op. Instr. 1.4.1.3)
Sawtooth phase meter	A	Adder, RF control Code error, mixer	Measuring error for f > f3 (see Op. Instr. 1.4.1.3) Jitter tolerance Code error detection
170 MHz LP filters	-	Code error	Jitter tolerance of code error detector
Mixer	GA	Code error	
Buffer stage 2	-	-	-
Code error (C)			
Code error 1 Code error 2	GA GA	- -	Jitter tolerance of code error detector
11 MHz circuit (E)			
11 MHz phase meter	A	Adder	Meaasuring error for f < f3 (see Op. Instr. 1.4.1.4)
Controller 1	GV	-	Locking, 11 MHz circuit, 2 Hz HP filter
11 MHz VCO	-	Controller 1	2 Hz HP filter
20:1 divider	A	-	-
11 MHz filter	A	-	-
Adder (F)	GV	-	Meas. error, freq. response
Filter (H)	A	-	-
Rectifier (K)	A	-	-
Hit counter (I)	GA	-	Counter threshold
RF control (G)	GA	-	Meas. error, freq. response
Display/control section (L)	Not applicable		
CPU-2A	Not applicable		

Fig. 4.6-1 Table: Effects of swapping individual circuits

Explanations to Table 4.6-1:

"Alignment" column:

Case "A": The board is completely aligned in advance; this board requires no further alignment in the instrument.

Applies for: - Installation of an aligned replacement board
- Installation of a board from a reference instrument, e.g. during troubleshooting.

Case "G": Circuit alignment to be performed in the instrument.

GF: The instrument function is retained even without the specified circuit alignment, but the restrictions stated alongside then apply.

GV: Like "GF", but settings must be made on the board beforehand, e.g. switch settings, trimmer settings (e.g. adder, controller 1).

GA: Instead of alignment in the instrument, preliminary alignment can be performed, e.g. using a different instrument. In this case, "GF" applies for the overall instrument function. This is the case, for example, if circuits from a different instrument are installed for troubleshooting purposes.

Note on case "GA":

In cases where instrument alignment is not possible, the instrument functions can be retained by installing a pre-aligned "GA" board, if the resultant restrictions have only a minor effect on the measuring task, if any.

"Restrictions if alignment not performed" column:

This column lists all restrictions of the instrument functions resulting from swapping of circuits if the alignments subsequently necessary in the instrument are not performed.

"Other circuits to be aligned" column:

It should be noted that, even after swapping case "A" boards, it may also be necessary to perform alignments on other boards. This column provides the necessary details.

General note:

The information provided here is only intended as assistance for troubleshooting in the overall instrument. For further details, see Section 7.1.1.

4.7 SPECIAL TEST SETUPS

4.7.1 INHERENT JITTER MEASUREMENT, 11 MHz CIRCUIT

Circuits covered by the measurement:

- 11 MHz VCO [2019-J]
- 11 MHz phase meter [2019-G]
- Controller 1 [2019-H]
- 20:1 divider [2019-AM]
- 11 MHz filter [2019-AN]

The following are measured:

1. Inherent jitter with controlled 11 MHz VCO, Section 4.7.1.1
2. Inherent jitter with free-running 11 MHz VCO, Section 4.7.1.2

Note: Measure with controlled 11 MHz VCO first. Only if excessive inherent jitter is found should the second measurement also be performed for further fault localization.

Preconditions:

- Inherent jitter of adder and evaluation circuit (filter/rectifier) tested and ok (see Section 4.5.3.3)
- 11 MHz circuit functional

Jitter display:

Display = Inherent jitter (11 MHz circuit + adder + evaluation circuit)

Instruments required:

- 220 MHz generator

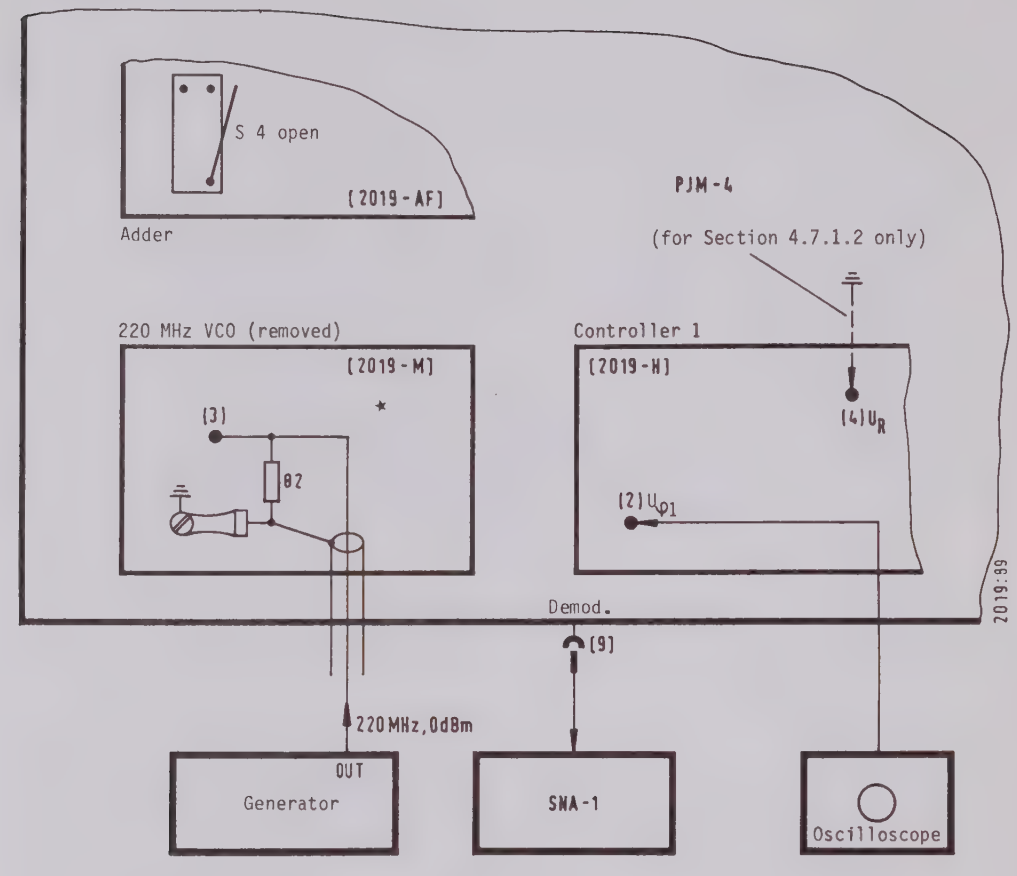
  Requirement: Low phase noise, e.g. Racal Dana, R & S SMG
  For Measurement 1, a good 220 MHz fixed-frequency source will also suffice.
  For Measurement 2, a synthesizer with 1 Hz resolution is essential.

- Oscilloscope, universal, e.g. Hameg
- Analyzer, e.g. SNA-1, if spectral analysis required

Software aid:

- "ENTW" test menu (see Sections 9.3 and 9.3.1)

Test setup:



Always observe the following (or the inherent jitter is increased!)

1. Do not apply an input signal
2. The 11 MHz VCO must be fitted with the cover
3. Protect the 11 MHz phase meter from strong draughts (e.g. fan)

* Or use test device No. 43-2019/2019-6500.054.

Instrument settings:

Generator: - 220 MHz, 0 dBm

PJM-4:
- Adder: Note setting of switch S 4; open switch!
- Remove 220 MHz VCO and apply generator signal as per sketch*.
- Call up testprogram BASIC NOISE (see section 4.5.3.1)
- Bit rate: Highest permanently installed bit rate (usually 139 Mbit/s)
- HP/LP filters: Any setting for jitter assessment.
  Pre-setting: HP = 2 Hz, LP = 600 kHz
- Select "ENTW" test menu

Oscilloscope:
- DC input, 0.5 V/DIV
- Position sawtooth oscillation with approx. 2.5 V_{pp} and +4 V DC offset in middle of display.

* Note: Do not use test device 20-2019 to apply the signal, since interference lines may occur if the 220 MHz signal is applied at Pt. (3) and Pt. (5):
$f_g = f_{bit\ rate} - n \times 11\ MHz$
where $f_g < 11$ MHz.

4.7.1.1 Inherent jitter measurement, controlled 11 MHz circuit

Measuring sequence:

1. Suppress the "NO SIGNAL" message:
   In the "EING. STUFE" test menu, set:
   EINGANGSTEILER 10 dB
2. Set the 11 MHz circuit:
   In the "REGELKREISE" test menu, set:
   RASTHILFE AUS
   REGLER 1 FREI, FLINK
3. Lock in the 11 MHz circuit:
   RAST-DAW TEST EIN
   When the sawtooth oscillation disappears from the oscilloscope: RAST-DAW STOP
   If the circuit remains locked in, select REGLER 1, TRAEGE
   The inherent jitter measurement is only correct with this setting!
4. Jitter measurement and evaluation:
   Press the "RETURN" key to return to the measuring program:
   Jitter display = Inherent jitter of 11 MHz circuit (+ inherent jitter of meas. circuit)
   The spectral components can be distinguished by selecting the HP and LP filters appropriately. Possibly examine with analyzer (in case of interference lines).

4.7.1.2 Inherent jitter measurement, 11 MHz circuit, with uncontrolled 11 MHz VCO

Measuring sequence:

1. Make the settings described in Section 4.7.1.1, Items 1 and 2 (essential!).
2. Clamp the 11 MHz VCO:
   Make a short connection between Pin 4 in controller 1 and ground.
3. Press the "RETURN" key to return to the measuring program.
4. Observe the sawtooth oscillation on the oscilloscope (symmetrical about the zero line). Tune the synthesizer, lastly in 1 Hz steps until the beating in the region of the zero line ceases.
5. Read the jitter display ≅ Inherent jitter
   As the 11 MHz VCO drifts, the synthesizer must be re-tuned frequently. However, slight phase drift has no effect on the inherent jitter display. When correcting the frequency, wait for the instrument to settle before reading the jitter display.
   Note: The 11 MHz VCO should have warmed up, since the frequency drift is otherwise too great for this measurement.

4.7.2 INHERENT JITTER MEASUREMENT, 220 MHz CIRCUIT

Circuits covered by the measurement:

- Input section (B) [2019-V]
- Sawtooth phase meter [2019-O]

The following are measured:

1. Inherent jitter for clock signals (test setup 1)*
2. Inherent jitter for data signals (test setup 2)*

Measuring procedure:

Feed the sawtooth phase meter from the same signal source. Split the signal via a power splitter (Measurement 1) or by separate tapping (Measurement 2). Feeding from a single signal source largely isolates its inherent jitter component. The sampling circuit of the phase meter receives its signal via the input circuit (and is thus also tested), the sawtooth circuit being fed directly.

Phase alignment:

For correct measurement, it is essential that sampling takes place on the correct, falling edge of the sawtooth oscillation. Under ideal circumstances, this corresponds to a 180° phase relation of the signals at the phase meter input. 180° inversion takes place in the input section.

The delay caused in the sampling circuit by the input section is compensated for by selecting the correct cable lengths (Measurement 1). In Measurement 2, there are additional mode-dependent phase/delay differences between the SIGNAL and REF. CLOCK outputs of the PJG-4, which may need to be compensated for.

---

* Preconditions: - Inherent jitter of evaluation circuit (filter/rectifier) tested and ok (see Section 4.5.3.3)

Instruments required, test setup 1:

- Oscilloscope: universal, e.g. Hameg
- 75 Ω cable 1 m (Cable I)
- 75 Ω cable 2.5 m (Cable II)
- 75 Ω cable 0.25 m
- 1 x 75 Ω T-adapter, a = 6 dB
- 1 x BNC T-adapter
- Test device 40-2019/2019-6500.025
- Test device 42-2019/2019-6500.041
- Synthesizer: output frequency to match bit rate frequency to be tested.

  As an alternative to the synthesizer (with the limitation that slightly higher inherent jitter may be measured, max. approx. 4 mUI):
  PJG-4 (unmodulated, clock)
  PS-16/SNA-1 generator (0 dBm send level only)

- Possibly high-speed oscilloscope: BW ≥ 300 MHz for checking the phase

Test setup 1:

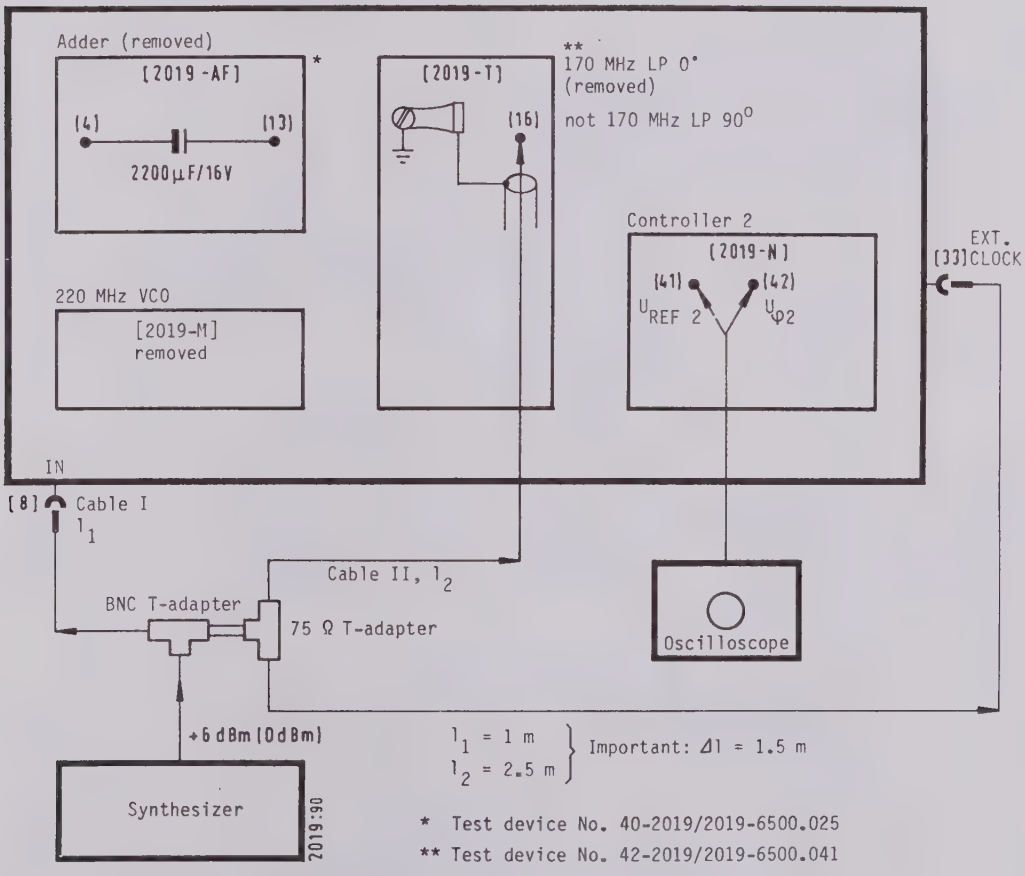


Fig. 4.7.2-1 Test setup for testing the inherent jitter for clock signals

Instrument settings, test setup 1:

PJM-4:
- Call up testprogram BASIC NOISE (see section 4.5.3.1)
- Bit rate: EXTERNAL
- Code: NRZ ECL
- Edge: LEADING EGDE!
- Set via "ENTW" test menu:
  "RASTHILFE EIN", then press "RETURN" key

Synthesizer:
- Level: +6 dBm (if possible)
  +0 dBm (possibly slightly higher inherent jitter, approx. 2 mUI)
- Frequency: As per desired bit rate frequency, for 139 MHz phase alignment (100 MHz also possible)

Oscilloscope:
- DC, 200 mV/DIV
- Pos. setting:
  Measure U_{Ref2} at 7 Pt. 41 in controller 2 (approx. 2.5 V DC) and position in the middle of the display
- Then connect test probe at 7 Pt. 42 ($U_{\varphi 2}$); do not change pos. setting any more, but check at regular intervals and correct, if necessary (Drift U_{Ref2}, Drift pos. setting).

Measuring sequence, measurement 1

1. Alignment of the phase relation:

a) Synthesizer frequency: 10 MHz
Check with the oscilloscope:
$U_{\varphi 2}$ (7 Pt. 42) = U_{Ref2} (7 Pt. 41) $\pm$ 20 mV
If the deviation is greater, check the test setup and instrument settings.
If ok, further instrument faults are likely, and the measurement is impossible.

b) Synthesizer frequency: 139 MHz (or 100 MHz)
$\Delta U_{\varphi 2} \leq$ 50 mV ($\Delta U_{\varphi 2} = U_{\varphi 2} - U_{Ref2}$)
If the deviations are greater, correct the cable lengths:
$\Delta U_{\varphi 2}$ pos.: Extend Cable I or shorten Cable II
$\Delta U_{\varphi 2}$ neg.: Shorten Cable I or extend Cable II
For this purpose: Δl = 10 cm $\cong$ $\Delta U_{\varphi 2} = \begin{cases} 50 \text{ mV (139 MHz)} \\ 36 \text{ mV (100 MHz)} \end{cases}$

2. Check of the phase relation:

a) At 139 MHz (100 MHz):
Position $U_{\varphi 2}$ at the middle of the display.
Alternately extend Cable I and Cable II with a 25 cm length. Observe the voltage jump $\Delta U_{\varphi 2}$:
Cable I + 25 cm: $\Delta U_{\varphi 2}$ = -130 mV (-95 mV)
Cable II + 25 cm: $\Delta U_{\varphi 2}$ = +130 mV (+95 mV)
If the voltage jumps measured deviate by more than 50%, or if they are in the wrong direction, this is due to incorrect alignment.

b) In case of uncertainty as to the phase relation, it can be checked with a high-speed oscilloscope in the pulse stages of the sawtooth meter:
CH 1 -> Collector 7 T 310 (sawtooth circuit)
CH 2 -> Collector 7 T 305 (sampling circuit)
φ_{CH2} = +180° $\pm$ 90°

3. Measurement:

- Press the "RETURN" key to return to the measuring program
- Select the weighting filter to suit the bit rate frequency
- Set the desired bit rate frequency on the synthesizer
- Determine the inherent jitter of the evaluation circuit:
  Connect Pt. (13) in the adder to ground via a 2200 µF capacitor: Display = Inherent jitter of evaluation circuit
- Use the 2200 µF capacitor to reconnect Pt. (13) <-> (4):
  Display = Inherent jitter (evaluation circuit + input section + sawtooth phase meter)
  Typical: Inherent jitter, input section + sawtooth phase meter ≤ Inherent jitter, evaluation circuit

Instruments required, test setup 2:

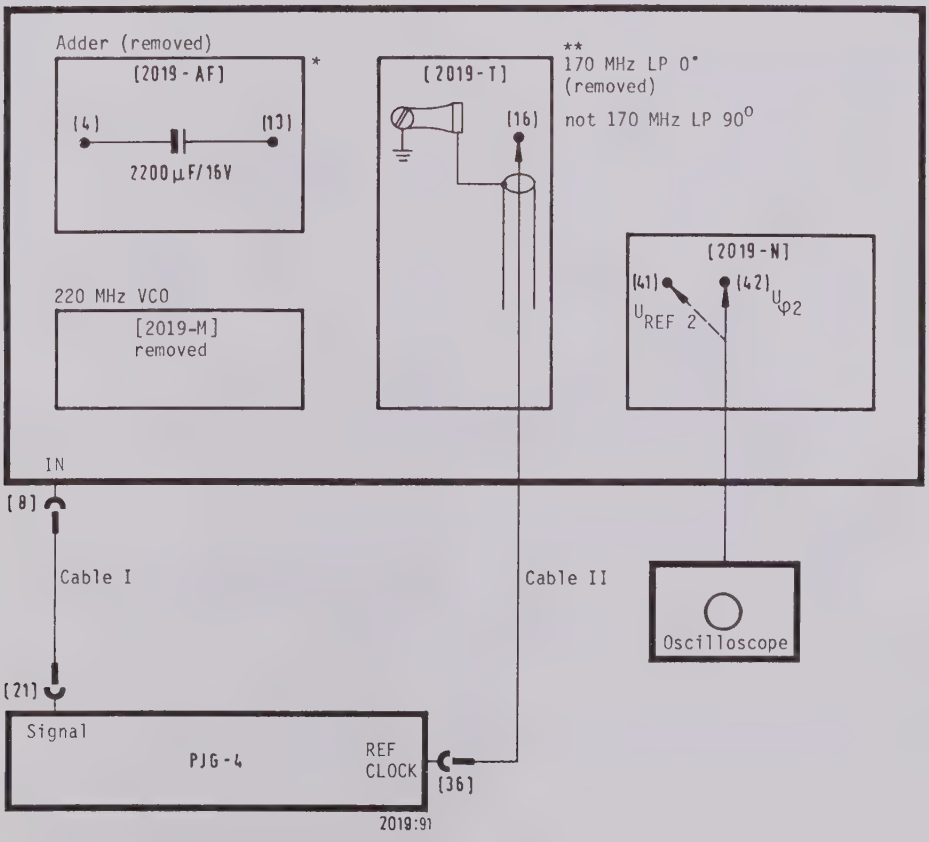
- Oscilloscope: universal, e.g. Hameg
- Cable I 75 Ω, e.g. 1 m
- Cable II 75 Ω, e.g. 2.5 m

} Cable lengths also depend on the PJG-4 used

Other lengths also possible.

- PJG-4: The inherent jitter should have been checked with a good PJM-4.

Test setup 2:



* Test device No. 40-2019/2019-6500.025

** Test device No. 42-2019/2019-6500.041

Fig. 4.7.2-2 Test setup for testing the inherent jitter for data signals

Instrument settings, test setup 2:

PJM-4: - Call up testprogram BASIC NOISE (see section 4.5.3.1)
- Bit rate
- Code
- Edge

} To match the desired test

- Set via "ENTW" test menu:
  "RASTHILFE EIN", then press the "RETURN" key

PJG-4: - Bit rate
- Code
- Data word/Random sequence

} To match the PJM-4 settings

- Modulation:
  INTERNAL : For phase check/alignment
  EXTERNAL : During measurement (not OFF, as this will cause a phase jump!)

Oscilloscope: As for test setup 1

Measuring sequence, test setup 2:

1. Check of the phase relation:

Set the instruments:
PJM-4: Bit rate, code, edge
PJG-4: Bit rate, code, data word
MOD. ~ , 20 kHz, 0.3 UI

If the phase relation is correct:
- Oscillation at 7 Pt. 42 not limited.
- Jitter display: 0.3 UI ± 0.05 UI

Possible remedy if one condition not fulfilled:
- Set other edge on PJM-4
- Only for 139 Mbit/s:
  Switch between MOD. OFF/Mod. ~ (possibly several times). The phase reversal then occurring between SIGNAL and REF. CLOCK can be used to obtain a suitable phase relation.
  Alternative possibility: Vary the cable lengths

2. Measurement:

Set Mod. EXTERNAL on the PJG-4 (not Mod. OFF, since this will cause a phase jump)
For measurement, see Item 3 in the measuring sequence for measurement 1.

4.7.3 TESTING THE CONTROL LIMIT FREQUENCY OF THE 220 MHz CIRCUIT

Measuring method:

First, the demod. level in the 220 MHz circuit for modulation frequencies above the control limit frequency (f_D) is determined with a modulation span of I_0 = 0.5 UI for use as a reference level.

The modulation frequency F_{mod} at which the demod. level is again equal to the reference level can then be determined with a modulation span of 10 x I_0 = 5 UI (ideally $f_{D\ nom}/10$).

The actual control limit frequency is then:

$f_D = 10 \times f_{mod}$

The measurement described below checks the level deviation from the reference level for

$f_{mod} = \frac{1}{10} \times f_{D\ nom}$.

Precondition:

- PJM-4 functional

Required instruments:

- PJG-4
- PS-19
- SPM-19

Test setup:

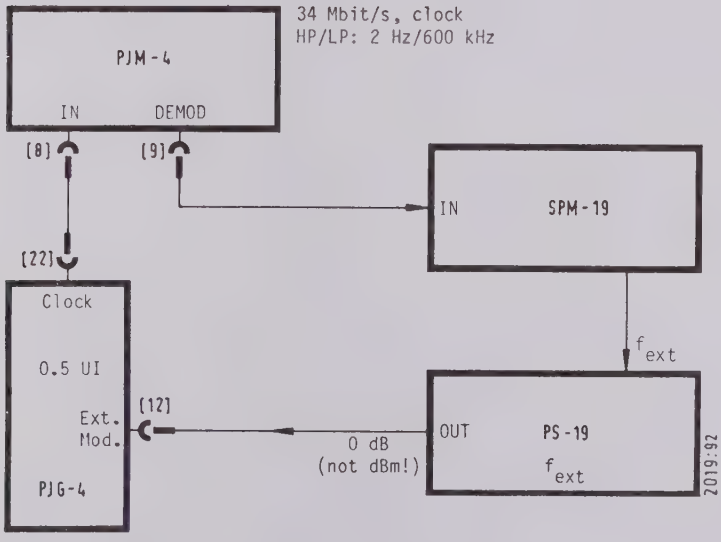


Fig. 4.7.3-1 Test setup for testing the control limit frequency of the 220 MHz circuit

Software aid:

- "ENTW" test menu (see Sections 9.3 and 9.3.1)
  Select the "CONTROL LIMIT FREQUENCY"* menu

  * "REGELGRENZFREQUENZ"

Instrument settings:

SPM-19: - 25 Hz bandwidth
- Digital display ABS
- 75 Ω input
- f = 100 KHz

PS-19: - Ext. frequency tuning
- Level = 0 dB
- 75 Ω output

PJM-4: - 34 Mbit/s, clock, NRZTTL
- HP = 2 Hz, LP = 600 KHz
- Switch over switch S 3 on the adder (11 MHz path OFF)
- Control limit frequency = 2 KHz S 3

PJG-4: - 34 Mbit/s, clock, TTL
- Ext. mod.
- 0.5 UI

Measuring sequence:

1. Determine and store the reference level:

- Measure the level in ABS mode at 100 KHz
  (measured value approx. 32 dB)
- Store: ABS -> REF
- Select ABS - REF mode (display: 0 dB ±0.1 dB)

2. Make the settings for the measurements:

PJG-4 : - 5 UI

3. Measurement:

Settings PJM-4 Control limit frequency	SPM-19 f	Limit test values	
6 kHz	0.600 kHz	+0.9 dB	-1.5 dB
12 kHz	1.2 kHz	+0.9 dB	-1.5 dB
25 kHz	2.5 kHz	+0.9 dB	-1.5 dB
60 kHz	6 kHz	+0.9 dB	-1.5 dB
150 kHz	15 kHz	+0.9 dB	-1.5 dB
240 kHz	24 kHz	+0.9 dB	-1.5 dB
500 kHz	50 kHz	+0.9 dB	-1.5 dB

4. Evaluation:

Limit value violation	Control limit frequency	Possible cause or 220 MHz VCO slope	Possible cause or Controller 2 gain	Remedy 7 R 415 in controller 2
+	Too low	Too small		Increase
-	Too high	Too large		Reduce

5. After measurement:

Set switch S 3 in the adder back to its original setting.

4.8 CIRCUIT-RELATED BLOCK CIRCUIT DIAGRAM

The circuit-related block circuit diagram at the end of this Service Manual is intended to assist in troubleshooting.

4.9 BOOTING

In the event of repairs, it may be necessary to disconnect the storage batteries, with the result that the stored data are lost. In order to reach a defined starting status, the instrument must be "booted" as follows:

1. Switch off the instrument.
2. Hold down the CLR key (on the front panel).
3. Switch on the instrument and hold down the CLR key until a short BEEP is heard.

The basic setting of the instrument can be found in Section 2.4 of the Operating Instructions.

5 TROUBLESHOOTING IN FUNCTIONAL GROUPS 5-1

5.1 Frequency generator (A) 5-1
5.1.1 Functional check of frequency generator 5-1
5.1.2 Troubleshooting in the event of exessive basic noise of the frequency generator. 5-2

5.2 Input circuit [2/2019-V] (B) 5-4
5.2.1 Functional check 5-4
5.2.2 Input circuit level diagram 5-9

5.3 Code error 1 and 2 [3/2019-AL], [4/2019-AO] (C) 5-10
5.3.1 Signal check 5-10
5.3.2 Code error display faulty 5-12
5.3.3 AIS display faulty 5-13

5.4 220 MHz circuit (D) 5-14
5.4.1 Signal and level check 5-14
5.4.2 Frequency response check, 220 MHz circuit 5-17
5.4.3 Troubleshooting in the event of lock-in problems in the 220 MHz circuit 5-18
5.4.3.1 Fault localization via the troubleshooting diagram in Section 4.5.2.2 5-18
5.4.3.2 Fault localization via the troubleshooting diagram in Section 4.5.2.3 5-19

5.5 11 MHz circuit (E) 5-20
5.5.1 Signal and level check, 11 MHz circuit 5-20
5.5.2 Frequency response check, 11 MHz circuit 5-23
5.5.2.1 Test the 2 Hz HP filter 5-23
5.5.2.2 Test the frequency response in the range up to 1 MHz 5-23
5.5.2.3 Test setup for measuring the frequency response of the 11 MHz circuit 5-24
5.5.3 Troubleshooting in the event of lock-in problems in the 11 MHz circuit 5-26
5.5.3.1 Fault localization via troubleshooting diagram in Section 4.5.2.2 5-26
5.5.3.2 Fault localization via troubleshooting diagram in Section 4.5.2.3 5-26
5.5.4 Troubleshooting in the event of exessive basic noise of the 11 MHz circuit 5-27

5.6 Adder [10/2019-AF] (F) 5-28
5.6.1 Control of signals and control voltages 5-28
5.6.2 Troubleshooting in the event of exessive basic noise 5-30
5.6.3 Frequency response check 5-32

5.7 RF control [14/2019-AF] (G) 5-34
5.7.1 Checking control voltage generation 5-34
5.7.2 Faulty address decoding 5-36

5.8 Filter/Rectifier [11/2019-Y/Z] (H/K) 5-37
5.8.1 Faulty jitter display 5-37
5.8.2 Faulty demod. signal 5-40
5.8.3 Faulty hit counter display 5-41
5.8.4 Level diagram, filter (11) and peak rectifier (12) 5-43
5.8.5 Timing diagram, peak rectifier 5-45

5.9 Hit counter [13/2019-AA] (I) 5-46
5.9.1 Functional check 5-46

5.10 Display/control section (L) 5-48
5.10.1 Functional check 5-48
5.10.2 Troubleshooting 5-50
5.10.2.1 Troubleshooting in voltage generator 5-50
5.10.2.2 Troubleshooting in multiplexer/column driver 5-51
5.10.2.3 Troubleshooting in the character generator/anode driver 5-52
5.10.2.4 Troubleshooting in the cursor driver 5-53
5.10.2.5 Troubleshooting in the computer core 5-54
5.10.2.6 Troubleshooting, command transfer 5-56
5.10.2.7 Troubleshooting, data transfer 5-57

5.11 Power supply unit (N) 5-58
5.11.1 Operating voltages 5-58
5.11.2 Troubleshooting in the power supply unit 5-58

5 TROUBLESHOOTING IN FUNCTIONAL GROUPS

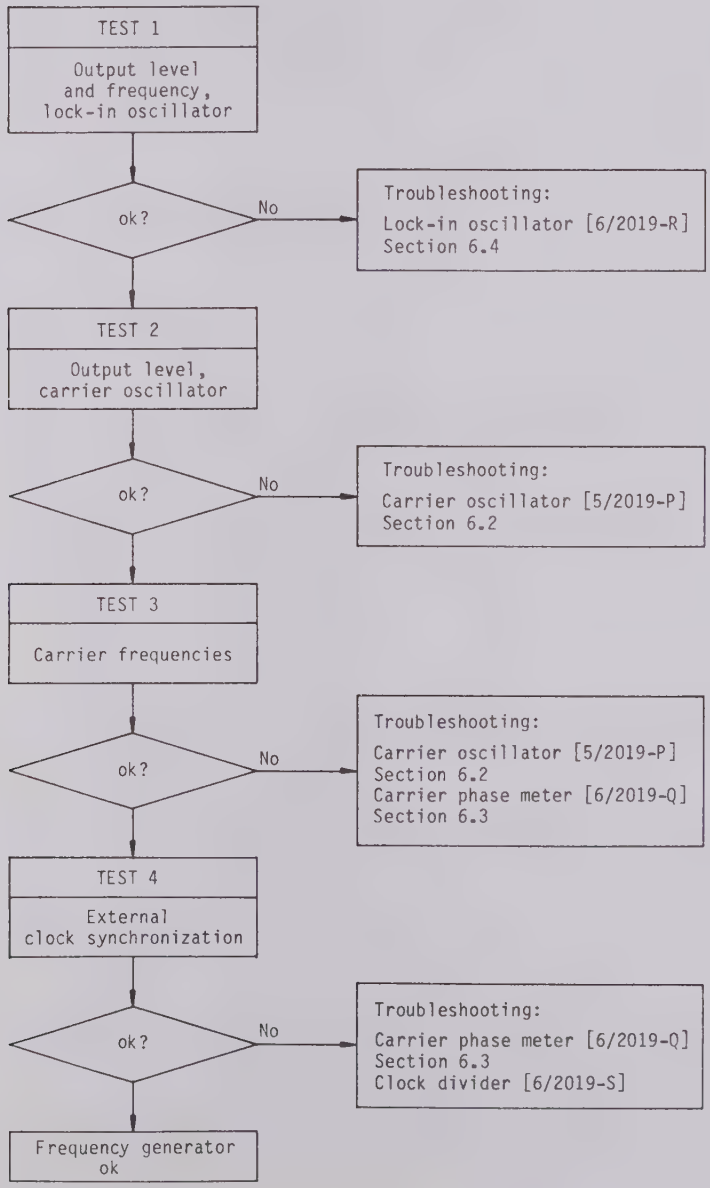
General notes

The circuit-related block circuit diagram at the end of the Service Manual provides assistance in troubleshooting.

The TEST X items entered in the circuit-related block circuit diagram refer to Section 5.

5.1 FREQUENCY GENERATOR (A)

5.1.1 FUNCTIONAL CHECK OF FREQUENCY GENERATOR



TEST 1: Lock-in oscillator [6/2019-R], output level and frequency

Operate the PJM-4 without an input signal

Connect an oscilloscope or frequency counter to 6 TP 16 in the lock-in oscillator.
Switch through all bit rates available in the PJM-4.

Level : Approx. 0.9 V_{pp} (3 dBm)
Frequency: Internal bit rate: 22 MHz + bit rate/10 ± 30 ppm
External bit rate: 22 MHz ± 30 ppm

TEST 2: Carrier oscillator [5/2019-P], output level

Operate the PJM-4 without an input signal

With an analyzer and active test probe (e.g. TEK P6201 and TEK 6201) at Pt. 16 and Pt. 20 in the oscillator, measure the level at all bit rates available in the PJM-4:

Level at (5) Pt. 20	Level at (5) Pt. 16	Perm. level range
Approx. 0 dBm (0.63 V_{pp})	Approx. -3 dBm (0.44 V_{pp})	-5 dBm ... +2 dBm

TEST 3: Carrier oscillator [5/2019-P], carrier frequency

Operate the PJM-4 without an input signal

Connect a frequency counter (e.g. Philips PM 6672) at Pt. 16 in the carrier oscillator.

Display value: 220 MHz + bit rate ± 30 ppm

TEST 4: External clock synchronization

Operate the PJM-4 without an input signal

Switch the PJM-4 to the EXTERNAL bit rate and connect the Ext. Clock input (33) on the PJM-4 (rear of instrument) to the level generator (e.g. PSS-16).
Generator level: 0 dBm

Connect a frequency counter (e.g. Philips PM 6672) at Pt. 16 in the carrier oscillator:

On the generator, set frequencies in the range from 0.7 (8 MHz for Series A PJM-4) to 168 MHz (160 MHz with PSS-16):

Display value: 220 MHz + generator frequency ± 30 ppm

5.1.2 TROUBLESHOOTING IN THE EVENT OF EXCESSIVE BASIC NOISE OF THE FREQUENCY GENERATOR

Precondition:

The troubleshooting diagram in Section 4.5.3.3 has been worked through, i.e. the limits for the inherent instrument jitter are complied with after completing TEST 5 (replacement of the frequency generator with a synthesizer):

--> The cause of the fault lies in the frequency generator

Further procedure:

- Using the SNA-1 analyzer and the test setup in Section 4.5.3.2, measure the spectrum of the frequency generator noise and compare it with Fig. 4.5-3.
- Use the notes in Table 4.5-5 to determine the type of jitter interference.
- Check whether the operating voltage interference is within the permitted range.

Further troubleshooting for:

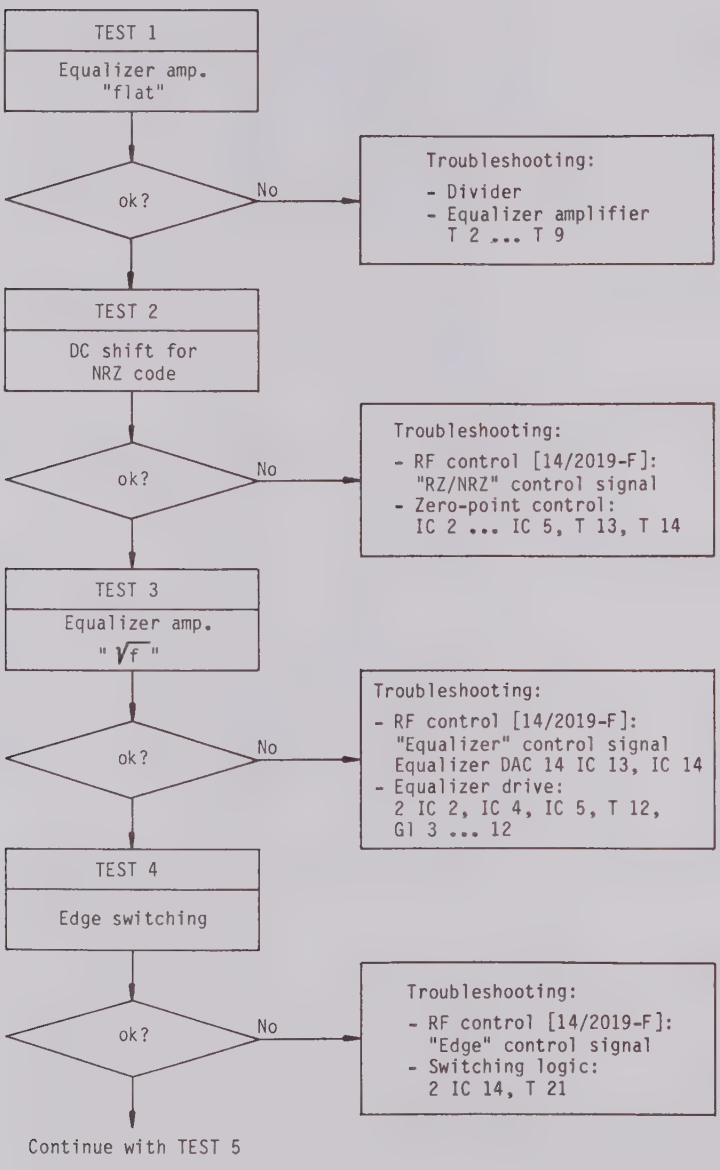
- Low-frequency jitter interference: Section 6.4 Lock-in oscillator [6/2019-R]
- Noise, increased noise : Section 6.3 Carrier phase meter [6/2019-Q]
  (compared with Fig. 4.5-6)

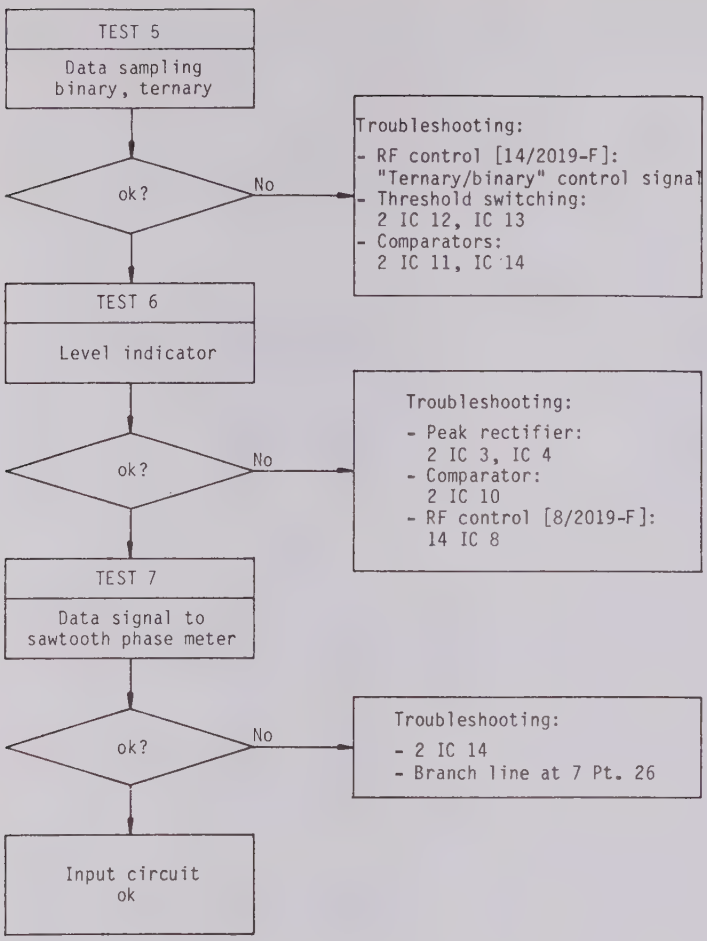
NOTE:

The carrier oscillator [5/2019-P] is not tested, as it has been removed. It must be considered as a possible fault source if the above tests fail to detect a fault.

5.2 INPUT CIRCUIT [2/2019-V] (B)

5.2.1 FUNCTIONAL CHECK



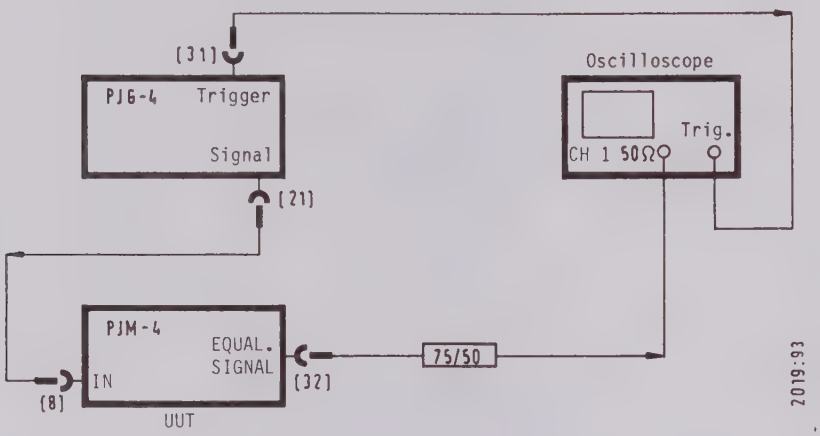

TEST 5
Data sampling binary, ternary
ok?
No
Troubleshooting:
- RF control [14/2019-F]: "Ternary/binary" control signal
- Threshold switching: 2 IC 12, IC 13
- Comparators: 2 IC 11, IC 14
TEST 6
Level indicator
ok?
No
Troubleshooting:
- Peak rectifier: 2 IC 3, IC 4
- Comparator: 2 IC 10
- RF control [8/2019-F]: 14 IC 8
TEST 7
Data signal to sawtooth phase meter
ok?
No
Troubleshooting:
- 2 IC 14
- Branch line at 7 Pt. 26
Input circuit ok

Test setup for functional check and input circuit:

Instruments required:

1 Jitter generator	PJG-4	W&G
1 Oscilloscope with 50 Ω input	e.g. 2465	Tektronix
1 Matching pad, 50/75 Ω	ZA 5075/BN 925	W&G
1 Attenuator, 10 dB	DG 1010	W&G

Test setup:



Settings: - PJG-4: CMI, 139 Mbit/s
Jitter mod. OFF
Bit pattern 1 ... 16 1100 1100 1100 1100 sequence

- PJM-4: Basic setting (Reset):
Hold down "Clear" key at power-up

TEST 1: Equalizer amplifier "flat"

On the PJM-4, use the "ENTW" test menu (see Section 9.3) to set the input divider to 20 dB in the "EINGANGSSTUFE" menu.

Check the signal at Bu 2 output [32] "EQUAL. SIGNAL" with the oscilloscope:

150 ... 250 mV_{pp}, no DC voltage component

TEST 2: DC shift for NRZ code

On the PJM-4, set: Code ECL/NRZ
Input divider 20 dB

Check the signal at Bu 2 output [32] "EQUAL. SIGNAL" with the oscilloscope:

Signal : 150 ... 250 mV_{pp}
Signal level "Low": 0 V

TEST 3: Equalizer amplifier " $\sqrt{f}$ "

on the PJM-4, set: Code CMI
$\sqrt{f}$ [4]

PJM-4 display : NOMINAL AMPLITUDE 0.50 V_p

Insert the 10 dB attenuator in the signal path

Check the signal at Bu 2 output [32] "EQUAL. SIGNAL" with the oscilloscope:

Signal : 150 ... 250 mV_{pp} (severe overshooting of the 140 MHz signal components)

TEST 4: Edge switching

On the PJM-4, set: Flat [4]
Edge: LEAD [4] or TRAIL
Remove attenuator

Measure the data signal at [32] Bu 2

Data signal at [32] Bu 2

Connect the oscilloscope to 2 IC 14, Pin 6 (ground, Pin 9) of the input circuit and measure the data signal with a 500 Ω test probe

Data signal EDGE LEAD

Data signal EDGE TRAIL

TEST 5: Data sampling, binary, ternary

On the PJM-4, set: Code: CMI
Edge: TRAIL [4]

Measure the signals DA^+ and DA^- in the input circuit with the test probe:

	Signal DA^+/2 Pt. 11	Signal DA^-/2 Pt. 10
Required	Signal as at [32] Bu 2 Amplitude approx. 400 mV_{pp}	DC approx. -0.9 V

On the PJM-4, set: 34.368 Mbit/s, code: AMI
34.368 Mbit/s, code: AMI

Measure the signals DA^+ and DA^- in the input circuit with the test probe:

	Signal DA^+/2 Pt. 11	Signal DA^-/2 Pt. 10
Required	Positive pulses of the signal at output [32] Bu 2 Amplitude: approx. 400 mV_{pp}	Negative pulses of the signal at output [32] Bu 2 Amplitude: approx. 400 mV_{pp}

TEST 6: Level indicator

1. Operate the PJM-4 without an input signal:

   The display must indicate "NO SIGNAL"

2. Settings: PJG-4 34.368 Mbit/s, code: AMI
   PJM-4 34.368 Mbit/s, code: CMI (!)
   $\sqrt{f}$ [4], enter nominal amplitude = 0.3 V

   The display must indicate "INPUT OVERLOAD"

TEST 7: DATA signal to the sawtooth phase meter

Feed an 8.448 Mbit/s clock signal to the PJM-4

Use the oscilloscope (BW > 300 MHz) with test probe and earth spring to check the pulse signal:

	2 Pt. 13 (input circuit)	or	7 Pt. 26 (sawtooth phase meter)
t_i	Approx. 5 ns		Approx. 3 ns
u_{pp}	Approx. 800 mV_{pp}		Approx. 400 mV_{pp}

Troubleshooting: - If no signal : Input circuit faulty
- If square-wave signal: Check branch line at 7 Pt. 26

5.2.2 INPUT CIRCUIT LEVEL DIAGRAM

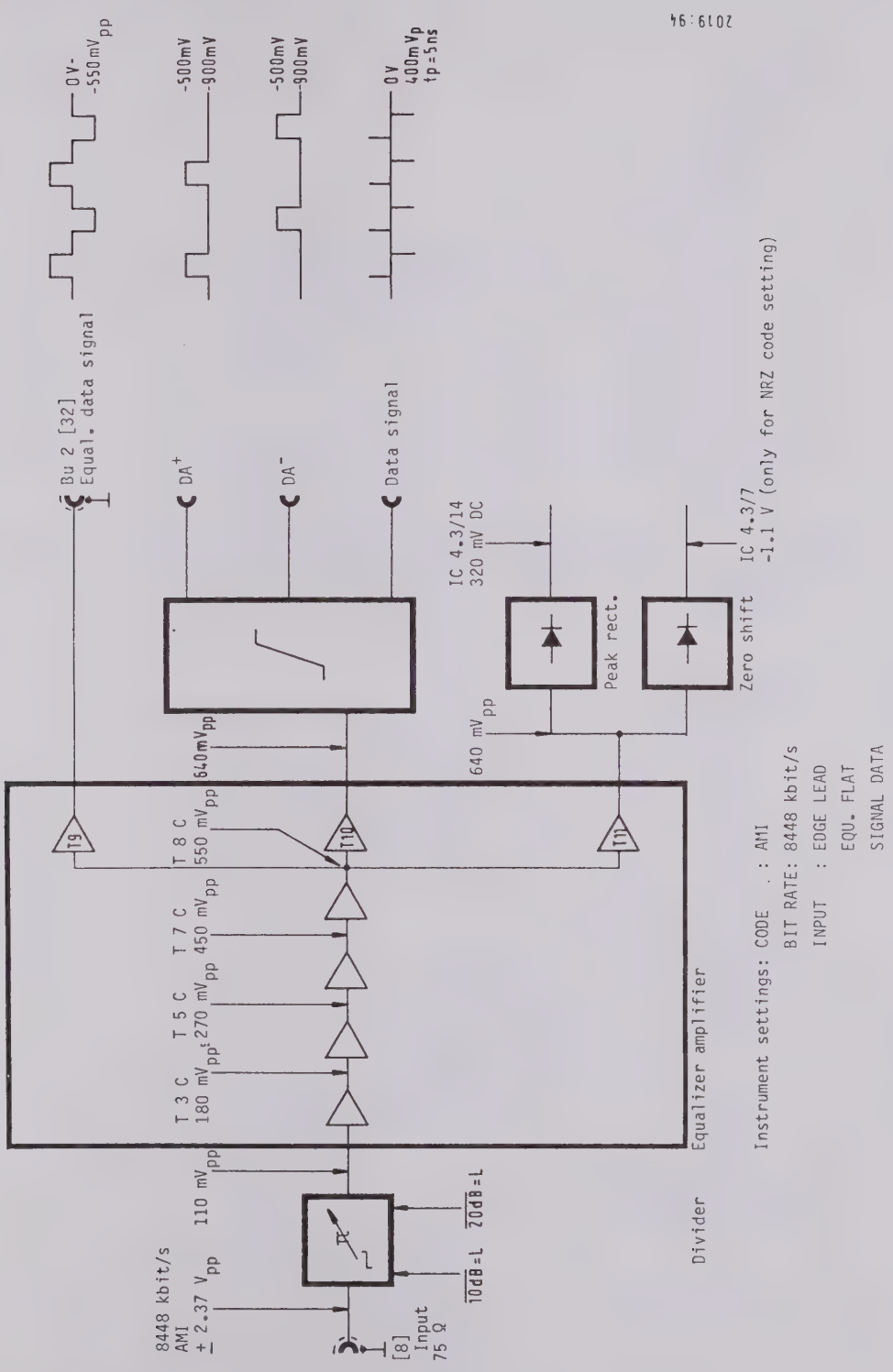
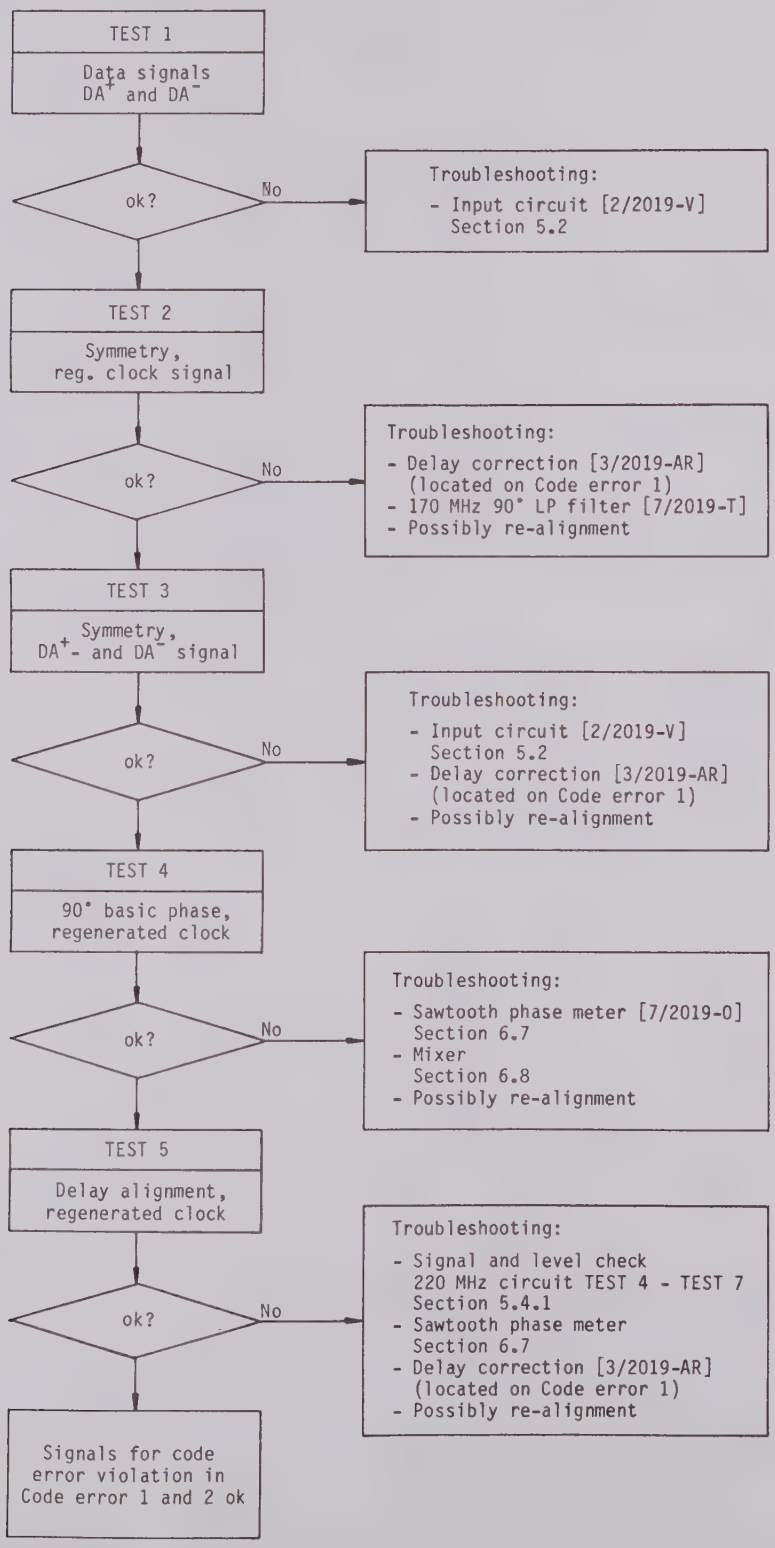


Fig. 5.2-1 Input circuit level diagram

5.3 CODE ERROR 1 AND 2 [3/2019-AL], [4/2019-AO] (C)

5.3.1 SIGNAL CHECK



TEST 1: Data signals DA^+ and DA^-

Check as per Section 5.2.1:
Carry out TEST 5 (data sampling, binary, ternary) with the test setup specified there

For further checks, see Section 9.2.3.1 in the circuitry description:

- For CMI : Fig. 9.2-8
- For HDB3 : Fig. 9.2-14
- For AMI : Fig. 9.2-13

TEST 2: Symmetry, reg. clock signal

Check as per alignment instructions in Section 7.2.3.1.1

TEST 3: Symmetry, DA^+- and DA^- signal

Check as per alignment instructions in Section 7.2.3.1.2/.3

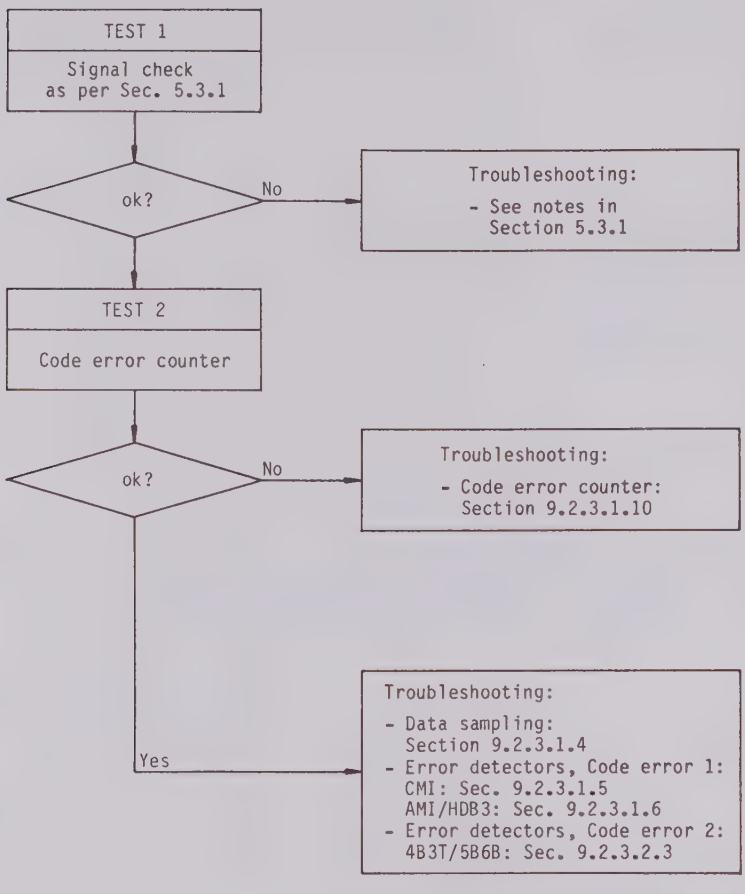
TEST 4: 90° basic phase, regenerated clock

Check as per alignment instructions in Section 7.2.3.1.1

TEST 5: Delay alignment, regenerated clock

Basic delay alignment : Check as per alignment instructions in Section 7.2.3.1.5
Bit rate-dependent delay: Check as per alignment instructions in Section 7.2.3.1.6

5.3.2 CODE ERROR DISPLAY FAULTY



TEST 2: Code error counter

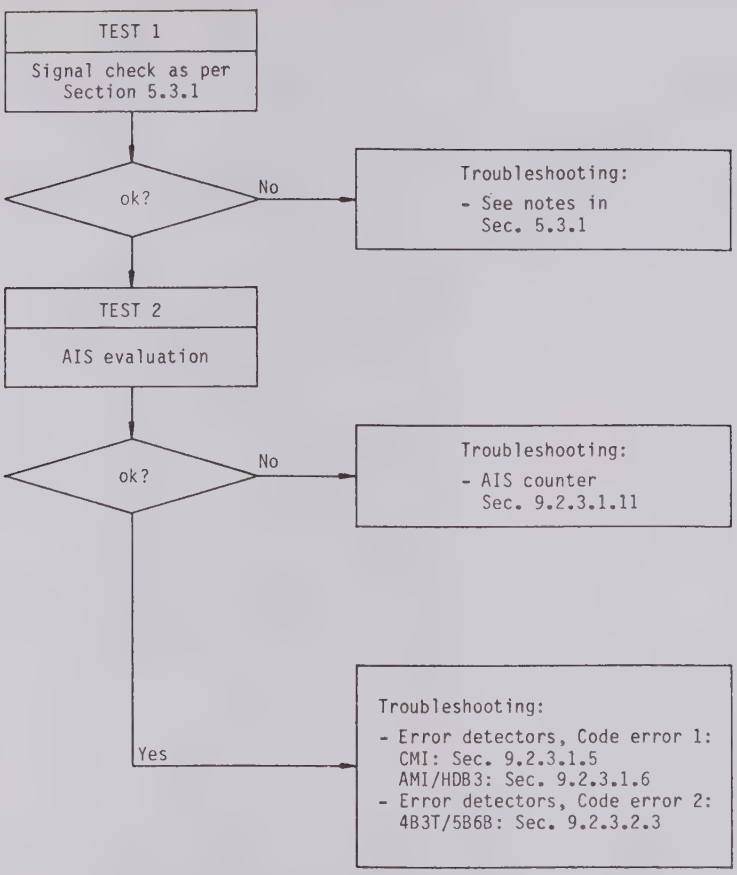
Synchronize the PJM-4 with any bit rate

Feed in a signal of known frequency at "CODE ERROR EXTERNAL" input [24].
Note: Use switch [22] to adjust the input to the generator level.

On the PJM-4, set : CODE ERROR "EXTERNAL"
GATING: 1 s

Start the measurement [5]: The counter result should be the same as the generator frequency

5.3.3 AIS DISPLAY FAULTY



TEST 2: AIS evaluation

Switch off the PJM-4 and carry out the following:

With Code error 2 option : On Code error 2 [4/2019-A0], use a diode wired to ground to set the inputs 4 IC 4, Pin 4 and 5, to approx. -0.7 V (= "H" level)

Without Code error 2 option: Connect control line IN 1 (Pt. c 1 on the connector comb) to +5 V. Use a diode wired to ground to set plug contact DATA 2 (3 Pt. 6) to approx. -0.7 V (= "H" level)

Switch on the PJM-4 and synchronize it with any bit rate (clock). Select code "4B3T" in the operator menu (see note):

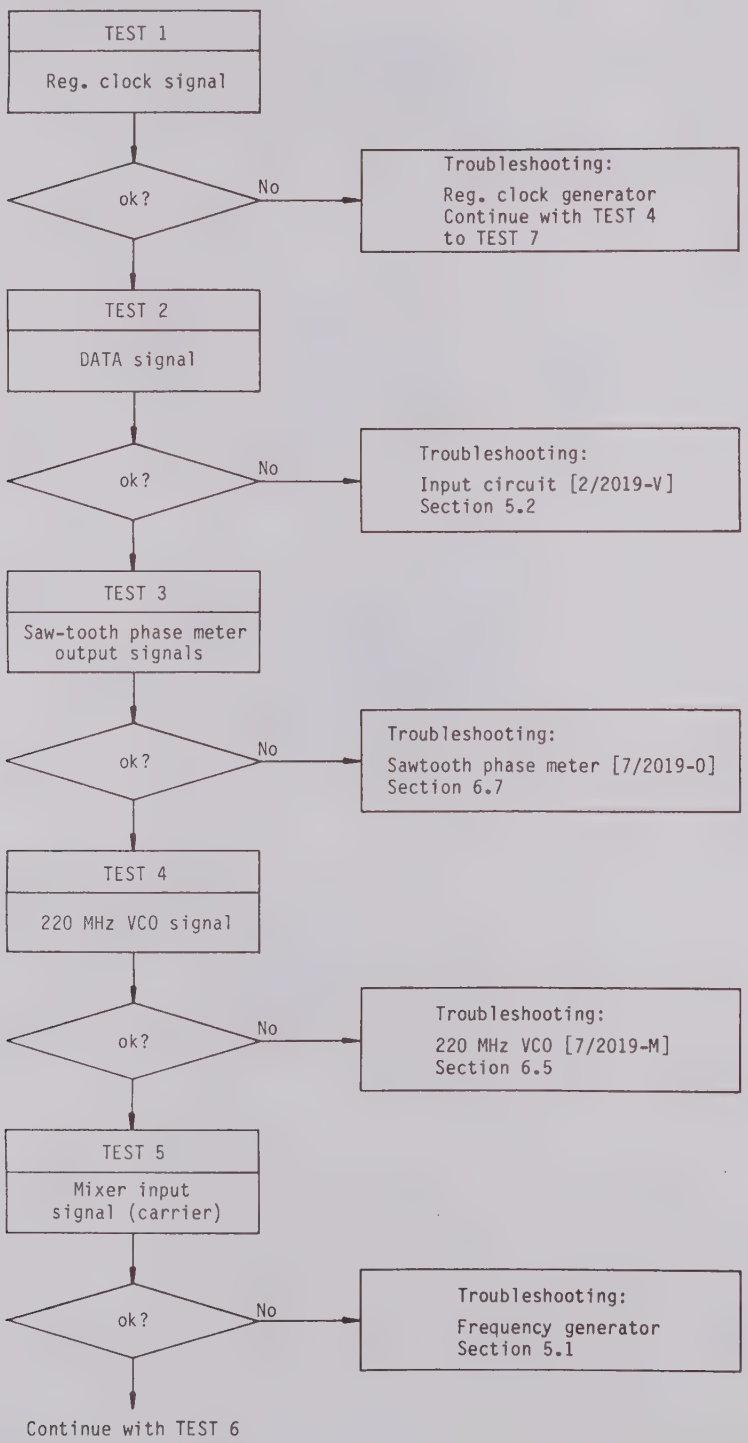
The AIS display should light up constantly.

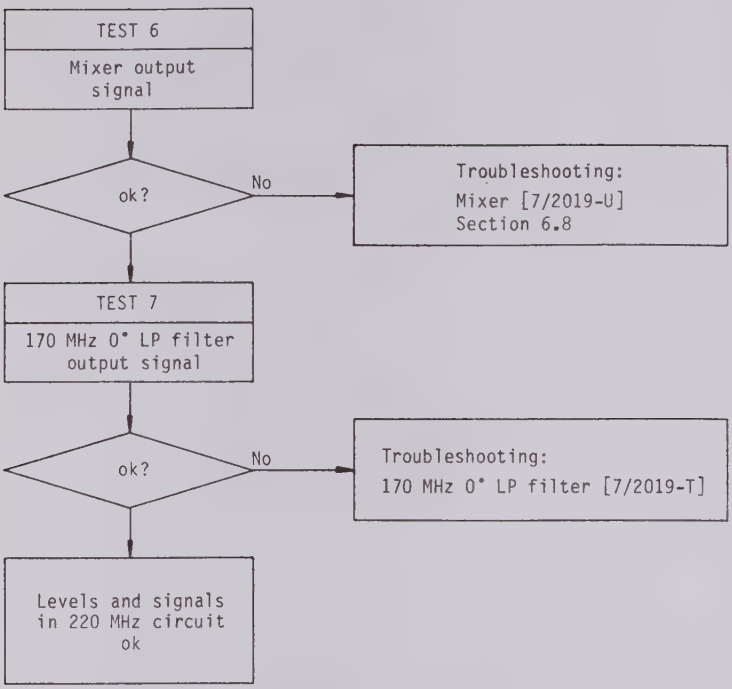
Note: The above conversions make the code setting "4B3T" selectable in the operator menu, even if it is not offered during normal operation of the instrument due to the absence of option 2.

Reverse the conversions after the test.

5.4 220 MHz CIRCUIT (D)

5.4.1 SIGNAL AND LEVEL CHECK





TEST 1: Regenerated clock

Measure the reg. clock signal in the 170 MHz 0° LP filter [7/2019-T] at Pt. 16 or in the saw-tooth phase meter [7/2019-0] at Pt. 31 in accordance with the specifications in TEST 7.

TEST 2: DATA signal

Test as per Section 5.2.1: Perform TEST 7

TEST 3: Saw-tooth phase meter [7/2019-0], output signals

Feed the PJM-4 with a clock signal from the PJG-4

For measuring in the non-locked state, open Dip-Fix switch 7 S 401 in (7) Controller 2 and connect the control voltage output Pt 46 to ground with a crocodile clip.
Measuring in the locked-in state is only carried out for checking, since locking-in is usually impossible in the event of a fault.

Measure in (7) Controller 2 (better access):

1. With oscilloscope, AC signal (sawtooth oscillation) at:

	7 Pt. 43 ($U_{\varphi 2}$)	Frequency
Locked-in	Crosstalk of sawtooth oscillation: < 100 mV_{pp}	Bit rate
Unlocked	Sampled sawtooth oscillation: 400 - 500 mV_{pp} Bit rate = 139 Mbit 630 - 770 mV_{pp} Bit rate < 35 Mbit	f < 100 kHz

2. With digital voltmeter, DC values at:

	7 Pt. 41 (U_{REF2})	7 Pt. 43 ($U_{\varphi 2}$)
Locked-in	1 ... 3 V	U_{REF2} ± 2 mV
Unlocked	1 ... 3 V	U_{REF2} ± 40 mV

3. Sawtooth oscillation at 2 Mbit/s setting (unlocked):

   Oscillation must not be limited.

TEST 4: 220 MHz VCO [7/2019-M]

Frequency: Test as per alignment instructions in Section 7.2.4.1.1
Level : Test as per alighment instructions in Section 7.2.4.1.2

TEST 5: Mixer input signal (carrier)

Test as per Section 5.1.1: Perform TEST 2 (carrier oscillator, output level)

TEST 6: Mixer output signal (reg. clock)

Operate the PJM-4 without an input signal

In (7) Controller 2, open Dip-Fix switch 7 S 401 and connect the control voltage output Pt. 46 to ground with a crocodile clip.

Select the bit rates available in the instrument consecutively. Use an analyzer and active test probe (e.g. SNA-1 and TK-11) to check the levels at points 8 and 9 in the mixer [7/2019-U]:

0° output, Pt. 8	90° output, Pt. 9	Perm. tolerance
Approx. -20 dBm	Approx. -12 dBm	± 4 dB

TEST 7: 170 MHz LP filter [7/2019-T], output signal

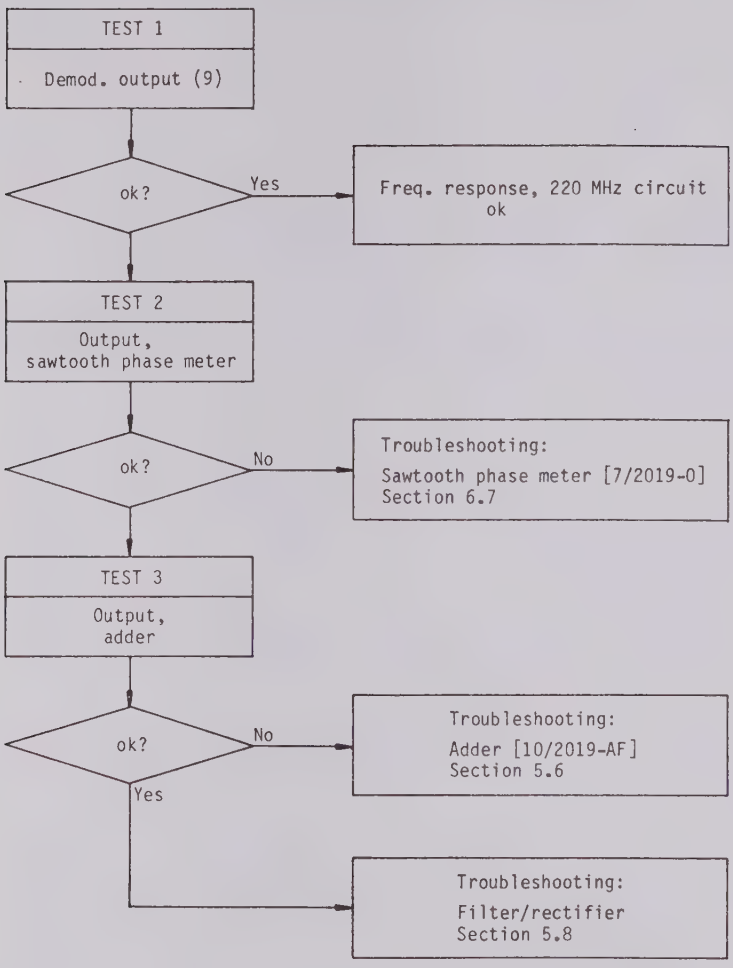
Operate the PJM-4 without an input signal

In (7) Controller 2, open Dip-Fix switch 7 S 401 and connect the control voltage output Pt. 46 to ground with a crocodile clip.

Select the bit rates available in the instrument consecutively. Use an analyzer and active test probe or oscillator (BW > 300 MHz) to check the levels at the outputs of the 170 MHz LP filters [7/2019-T] and a frequency counter to measure the regenerated clock frequency at one output:

0° LP filter Pt. 16/Pt. 18	90° LP filter Pt. 16/Pt. 18	Level tolerance	Frequency tolerance
Approx. -4 dBm	Approx. 0 dBm	± 4 dB	± 500 kHz

5.4.2 FREQUENCY RESPONSE CHECK, 220 MHz CIRCUIT



TEST 1: Frequency response, 220 MHz circuit to demod. output [9]

Establish the test setup as per Section 7.2.6 "Adder alignment".

Note: The housing of the PJM-4 need not be removed for this measurement. The switch settings in the adder remain unchanged!

On the PJM-4, use the test menu (see Section 9.3) to set the control limit frequency = 2 kHz.

Only carry out the measurement specified under "Check" in Section 7.2.6.5 for the individual bit rates and compare the results with the typical frequency responses in Fig. 7.2.6-3.

TEST 2: Frequency response, 220 MHz circuit to sawtooth phase meter output [7/2019-0]

Connect the SNA-1 with active test probe TK 11 to 7 Pt. 43 ($U_{\varphi 2}$) in Controller 2 [7/2019-N] (due to better accessibility).

The test setup and test sequence is as for TEST 1 in all other respects.

TEST 3: Frequency response, 220 MHz circuit to adder output [10/2019-AF]

Connect the SNA-1 with active test probe TK 11 to 10 Pt. 13 in the adder.

The test setup and test sequence is as for TEST 1 in all other respects.

5.4.3 TROUBLESHOOTING IN THE EVENT OF LOCK-IN PROBLEMS IN THE 220 MHz CIRCUIT

Precondition:

Initial fault localization performed as per the troubleshooting diagrams in Sections 4.5.2.2 and 4.5.2.3.

5.4.3.1 Fault localization via the troubleshooting diagram in Section 4.5.2.2

Fault in TEST 1: Reg. clock generator faulty

Troubleshooting:
- Perform TEST 4 to TEST 7 as per Section 5.4.1

Fault in TEST 3: Lock-in aid, 220 MHz circuit, faulty

Troubleshooting:
- Perform TEST 4 as per Section 5.4.1
- Test 11 MHz circuit as per Section 5.5.1
- Troubleshooting in Controller 2; Section 6.6

Fault in TEST 5: No output signal from 220 MHz circuit

Troubleshooting:
- Perform TEST 1 to TEST 3 as per Section 5.4.1

Fault in TEST 6: 220 MHz circuit fails to lock in

Troubleshooting:
- Perform TEST 2 and TEST 3 as per Section 5.4.1
- Check charging current $I_{\varphi 5}$ for sawtooth phase meter as per alignment instructions in Section 7.2.10.1
- Troubleshooting in Controller 2; Section 6.6

5.4.3.2 Fault localization via troubleshooting diagram in Section 4.5.2.3

Fault in TEST 1/2: 220 MHz circuit fails to lock in when modulated

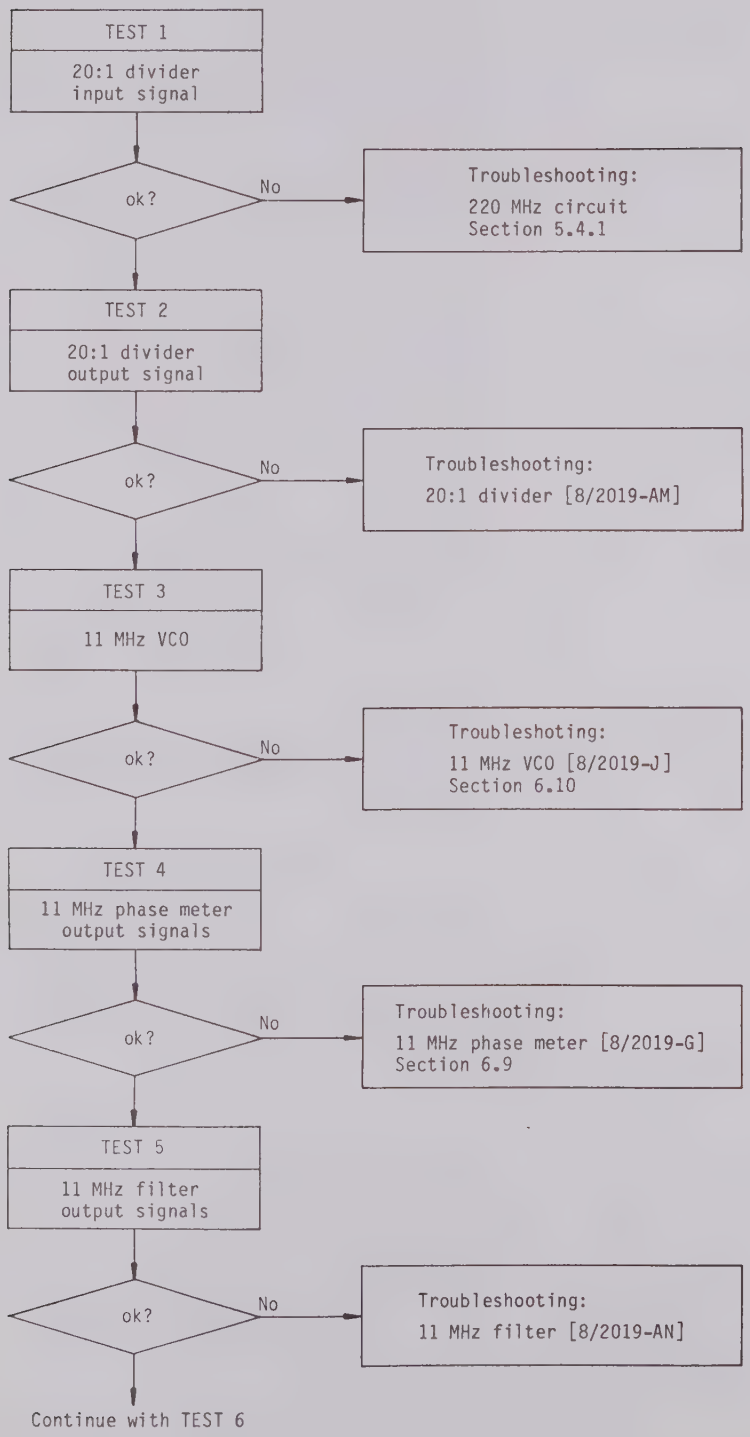
Troubleshooting:
- Perform TEST 3 as per Section 5.4.1
- Check the control limit frequency of the 220 MHz circuit as per Section 4.7.3 (if possible despite fault)
- Check Controller 2 (gain setting); Section 6.6

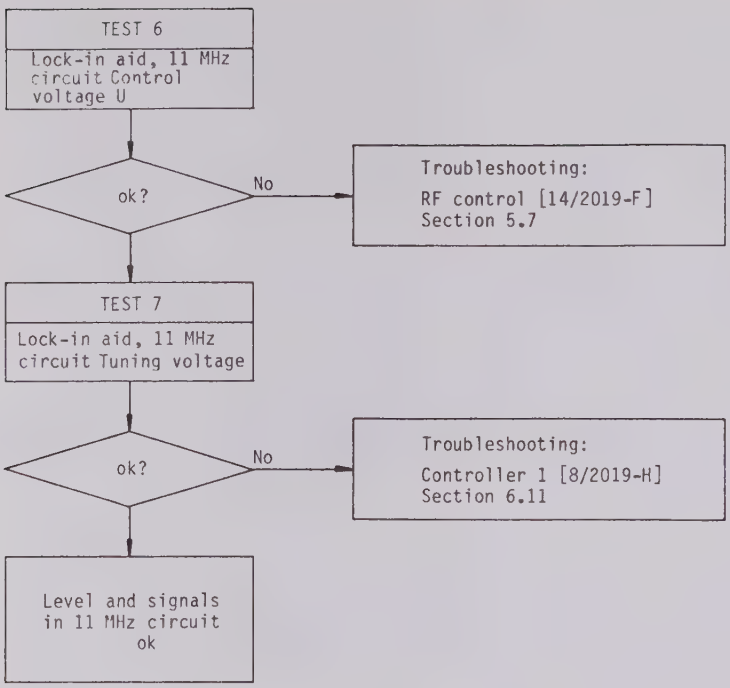
Fault in TEST 5 : Lock-in detector for 11 MHz circuit in Controller 2 faulty

Troubleshooting:
- Troubleshooting in Controller 2; Section 6.6

5.5 11 MHz CIRCUIT (E)

5.5.1 SIGNAL AND LEVEL CHECK, 11 MHz CIRCUIT




TEST 6
Lock-in aid, 11 MHz circuit Control voltage U
ok?
No
Troubleshooting:
RF control [14/2019-F]
Section 5.7
TEST 7
Lock-in aid, 11 MHz circuit Tuning voltage
ok?
No
Troubleshooting:
Controller 1 [8/2019-H]
Section 6.11
Level and signals in 11 MHz circuit ok

TEST 1: 20:1 divider input signal

Operate the PJM-4 without an input signal

In (7) Controller 2, open Dip-Fix switch 7 S 401 and connect the control voltage output for the 220 MHz VCO at 7 Pt. 46 to ground with a crocodile clip.

Use an oscilloscope (BW > 300 MHz) or frequency counter to measure at 8 Pt. 1 in the 20:1 divider [8/2019-AM]:

$U = 400\ mV_{pp}$ $\pm$ $100\ mV_{pp}$
$f = 220\ MHz$ $\pm$ 100 kHz

TEST 2: 20:1 divider [8/2019-AM], output signal

Operate the PJM-4 without an input signal

In (7) Controller 2, open Dip-Fix switch 7 S 401 and connect the control voltage output for the 220 MHz VCO at 7 Pt. 46 to ground with a crocodile clip.

Use an oscilloscope (BW > 300 MHz) or frequency counter to measure at 8 Pt. 3 in the 20:1 divider [8/2019-AM]:

$U = 800\ mV_{pp}$ $\pm$ $100\ mV_{pp}$
$f = 11\ MHz$ $\pm$ 5 kHz

TEST 3: 11 MHz VCO [8/2019-J]

Operate the PJM-4 without an input signal

In (9) Controller 1, connect the control voltage output 8 Pt. 4 to ground with a crocodile clip.

Use an oscilloscope (BW > 300 MHz) or frequency counter to measure at 8 Pt. 13 in the 11 MHz phase meter [8/2019-G]:

U = Approx. 1 V_{pp}
$f = 11\ MHz$ $\pm$ 1 kHz

TEST 4: 11 MHz phase meter [8/2019-G], output signals

Operate the PJM-4 without an input signal

In (7) Controller 2, open Dip-Fix switch 7 S 401 and connect the control voltage output for the 220 MHz VCO at 7 Pt. 46 to ground with a crocodile clip.

Use a DVM (e.g. Fluke 8050 A) to measure the DC levels at the following points in the 11 MHz phase meter [8/2019-G]:

8 Pt. 14 (U_{REF1})	4.2 V	$\pm$ 250 mV
8 Pt. 15 ($U_{\varphi 1}$)	1.3 x U_{REF1}	$\pm$ 260 mV

TEST 5: 11 MHz filter [8/2019-AN], output signals

Operate the PJM-4 without an input signal

In (7) Controller 2, open Dip-Fix switch 7 S 401 and connect the control voltage output for the 220 MHz VCO at 7 Pt. 46 to ground with a crocodile clip.

Use a DVM (e.g. Fluke 8050 A) to measure the DC levels at the following points in the 11 MHz filter [8/2019-AN]:

8 Pt. 23 (U_{REF1})	4.2 V	$\pm$ 250 mV
8 Pt. 24 ($U_{\varphi 1}$)	U_{REF1}	$\pm$ 200 mV

TEST 6: Lock-in aid, 11 MHz circuit, control voltage U_{LOCK}

Operate the PJM-4 without an input signal

Via the "ENTW" test menu (see Section 9.3), make the following settings in the "RAST-EINST" menu:

- REGLER 1 "FREI", "FLINK"
- RASTHILFE "AUS"
- RAST-DAW "TEST"

Use an oscilloscope to measure the control voltage at input Pt. 8 in Controller 1 [8/2019-H]:

The control voltage runs through the range from -7 V to +7 V in cyclic fashion.

TEST 7: Lock-in aid, 11 MHz circuit, tuning voltage

Operate the PJM-4 without an input signal

Via the "ENTW" test menu (see Section 9.3), make the following settings in the "RAST-EINST" menu:

- REGLER 1 "FREI", "FLINK"
- RASTHILFE "AUS"
- RAST-DAW "TEST"

Use an oscilloscope to measure control voltage 1 at Pt. 4 in Controller 1 [8/2019-H]:

The tuning voltage runs through the range from -7 V to +7 V in cyclic fashion.

5.5.2 FREQUENCY RESPONSE CHECK, 11 MHz CIRCUIT

5.5.2.1 Test the 2 Hz HP filter

The HP filter cutoff frequency is determined by the gain in the 11 MHz circuit and is normally aligned to 2 Hz.

Perform the check as per the alignment instructions in Section 7.2.5.4.1.

Troubleshooting: - Controller 1 (Sec. 6.11) : Gain fault
Faulty fast/slow switching
- RF control (Sec. 5.7) : Faulty fast/slow driver

5.5.2.2 Test the frequency response in the range up to 1 MHz

The frequency response of the 11 MHz circuit in the important range up to approx. 1 MHz cannot be tested during normal operation of the PJM-4.

Therefore, perform a check with the test setup as per Section 5.5.2.3 and compare the measured results with the typical frequency response in Fig. 5.5.2-1.

The deviation at 1 MHz as opposed to 1 kHz should not exceed 0.2 dB.

Troubleshooting: - 11 MHz phase meter (Section 6.9)
- 11 MHz filter

5.5.2.3 Test setup for measuring the frequency response of the 11 MHz circuit

In the following test setup, the 20:1 divider is removed and the 11 MHz circuit fed directly with a phase-modulated 11 MHz signal from the PJG-4.

Precondition: - Fully-functional PJM-4 (lock-in and display function)

Instruments:
- PJG-4
- SNA-1/02
- Active test probe TK 11
- PS-16 or other synthesizer with 44 MHz or 44 MHz fixed-frequency source
- Oscilloscope > 20 MHz

Software aid:
- "ENTW" test menu
- See Section 9.3

Test setup:

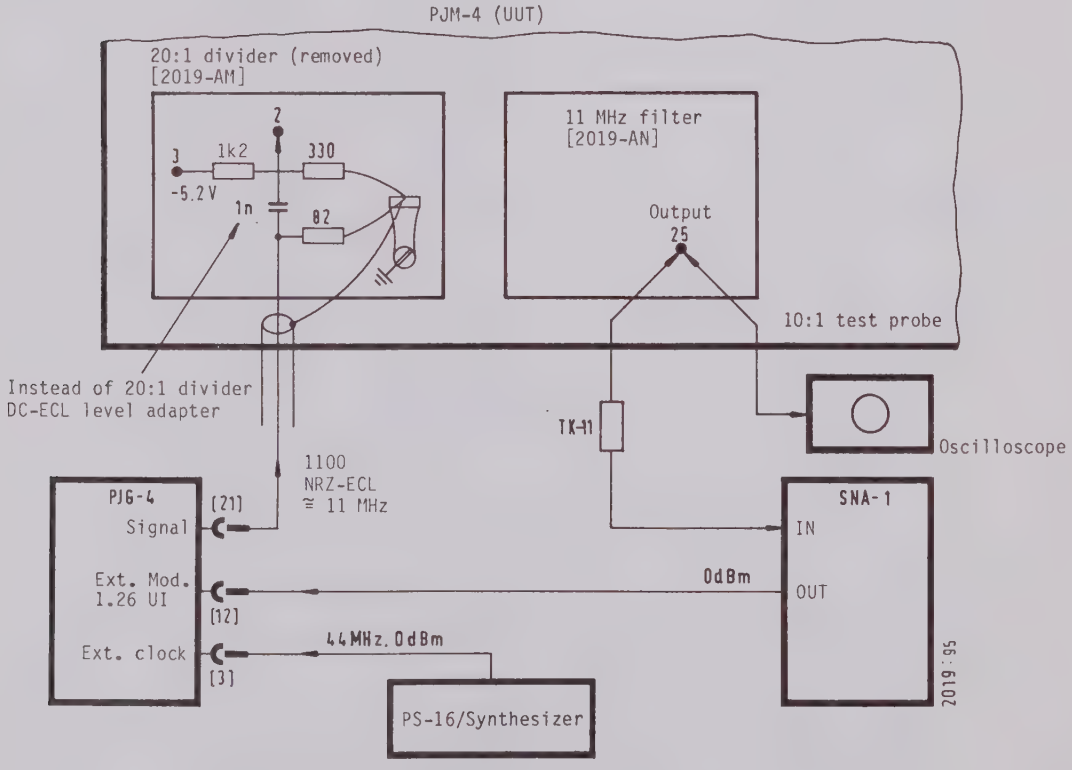


Fig. 5.5.2-1 Test setup for measuring the frequence response of the 11 MHz circuit

Instrument settings:

PJG-4
- Ext. mod. [13]
- 1.26 UI, range 0.1 ... 2.4 UI [5]
- Ext. clock [3]
- Output signal [21], NRZ-ECL [16]
- Pattern 1 ... 16 [15], sequence 1100

Synthesizer - 44 MHz, 0 dBm

PJM-4
- Do not apply an input signal
- Bit rate: EXTERNAL
- Select the "RAST-EINST" menu via the "ENTW" test menu

SNA-1
- Frequency range: 1 kHz ... 1 MHz, 3 decades
- Reference level: Approx. -9 dB
- See Fig. 5.5.2-2 for all other settings
- Normalization of the SNA-1 with the TK-11:
  Make the settings on the SNA-1; then connect the TK-11 to the PJG-4 input (using a T-adapter); do not break the connection PJG-4 - SNA-1 - Generator.
  Normalize the SNA-1.
  Check: At a reference level of 0 dB, the frequency response must be flat in the entire frequency range

Test sequence:

1. Lock in the 11 MHz circuit:
   - Set "Mod. OFF" on the PJG-4.
   - If the test setup is correct, a low-frequency sawtooth oscillation must be measurable (oscilloscope) at the output of the 11 MHz filter.
   - In the "RAST-EINST" menu, set: RASTHILFE "AUS"
     REGLER 1 "FREI"; "FLINK"
     RAST-DAW "TEST"
   - When the sawtooth oscillation disappears, set RAST-DAW "STOP" (circuit locked in).
   - Set "Mod. EXTERNAL" on the PJG-4.
     PJM-4: Set REGLER 1 "TRAEGE"; the circuit must remain locked in.

2. Frequency response measurement:
   Connect the TK-11 to the output of the 11 MHz filter.
   Possibly remove oscilloscope test probe. Also see Fig. 5.5.2-2.

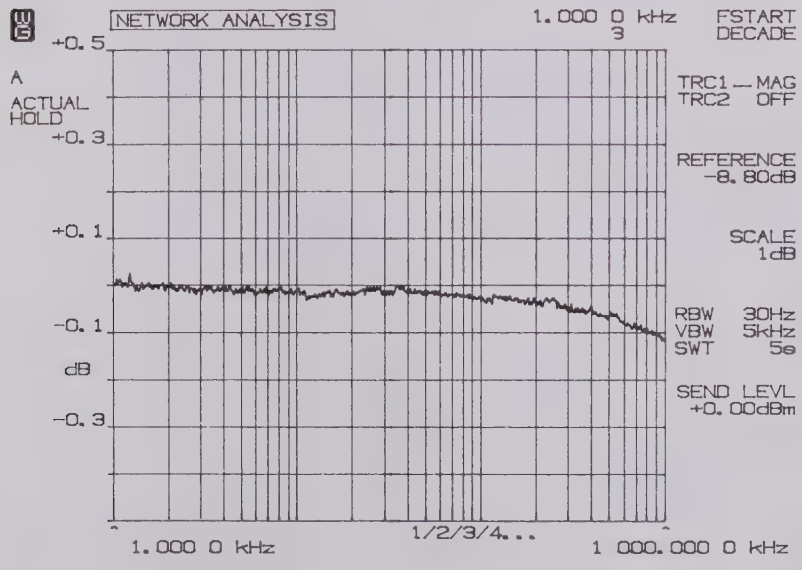


Fig. 5.5.2-2 Typical frequency response of the 11 MHz circuit

5.5.3 TROUBLESHOOTING IN THE EVENT OF LOCK-IN PROBLEMS IN THE 11 MHz CIRCUIT

Precondition: Initial fault localization must have been carried out as per the troubleshooting diagrams in Sections 4.5.2.2 and 4.5.2.3.

5.5.3.1 Fault localization via troubleshooting diagram in Section 4.5.2.2

Fault in TEST 2: No output signal from 11 MHz circuit

Troubleshooting:
- Test the 11 MHz circuit as per Section 5.5.1

Fault in TEST 3: Faulty lock-in aid, 220 MHz circuit

Troubleshooting:
1. Test the 11 MHz circuit as per Section 5.5.1
2. TEST 3 in Section 6.6 (Controller 2)

Fault in TEST 4: Excessive frequency deviation of reg. clock

Troubleshooting:
1. TEST 3 in Section 5.5.1 (11 MHz circuit)
2. TEST 2 in Section 6.11 (Controller 1)

Fault in TEST 8: Faulty tuning range of 11 MHz circuit

Troubleshooting as per Section 5.5.1:
1. TEST 3
2. TEST 6, TEST 7

Fault in TEST 9: 11 MHz circuit fails to lock in

Troubleshooting:
1. TEST 4, TEST 5 in Section 5.5.1
2. Troubleshooting in Controller 1, Section 6.11

5.5.3.2 Fault localization via troubleshooting diagram in Section 4.5.2.3

Fault in TEST 3: 11 MHz fails to lock in with jitter

Troubleshooting:
1. TEST 4, TEST 5 in Section 5.5.1
2. Troublesooting in Controller 1, Section 6.11

Fault in TEST 4: 11 MHz circuit unlocks following manaul "fast/slow" switching

Troubleshooting:
- TEST 3 in Section 6.11 (Controller 1)

Fault in TEST 5: Automatic "fast/slow" switching faulty

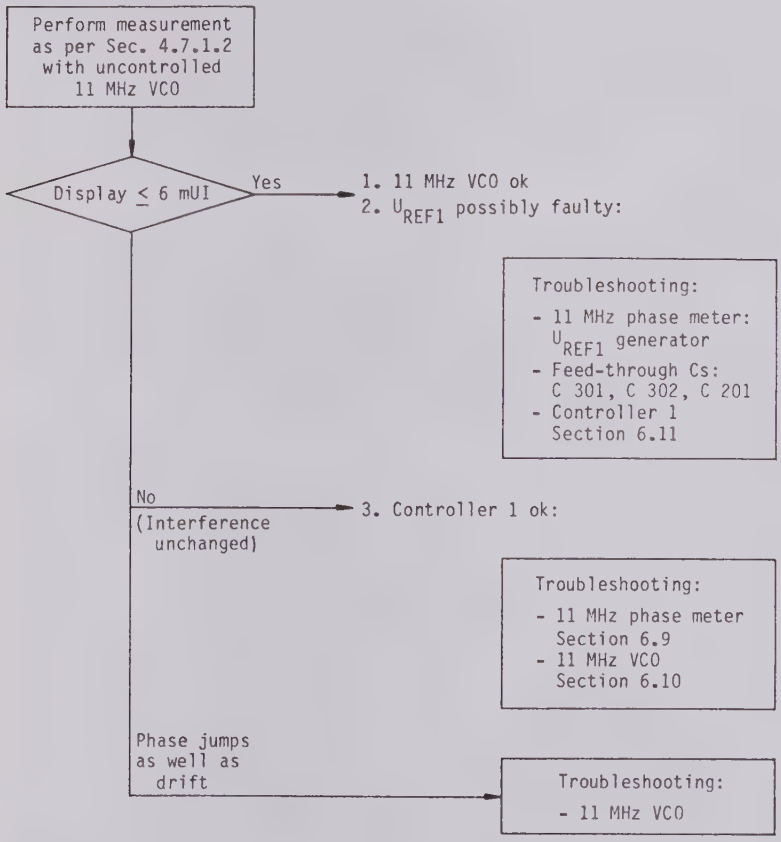
Troubleshooting:
1. Check lock-in aid alignment as per Section 7.2.5.4.3
2. Troubleshooting in Controller 1, Section 6.11

5.5.4 TROUBLESHOOTING IN THE EVENT OF EXCESSIVE BASIC NOISE OF THE 11 MHz CIRCUIT

Precondition: The troubleshooting diagram in Section 4.5.3.3 must have been worked through up to and including TEST 3:

Fault cause located in the 11 MHz circuit:
- 11 MHz VCO
- 11 MHz phase meter
- Controller 1

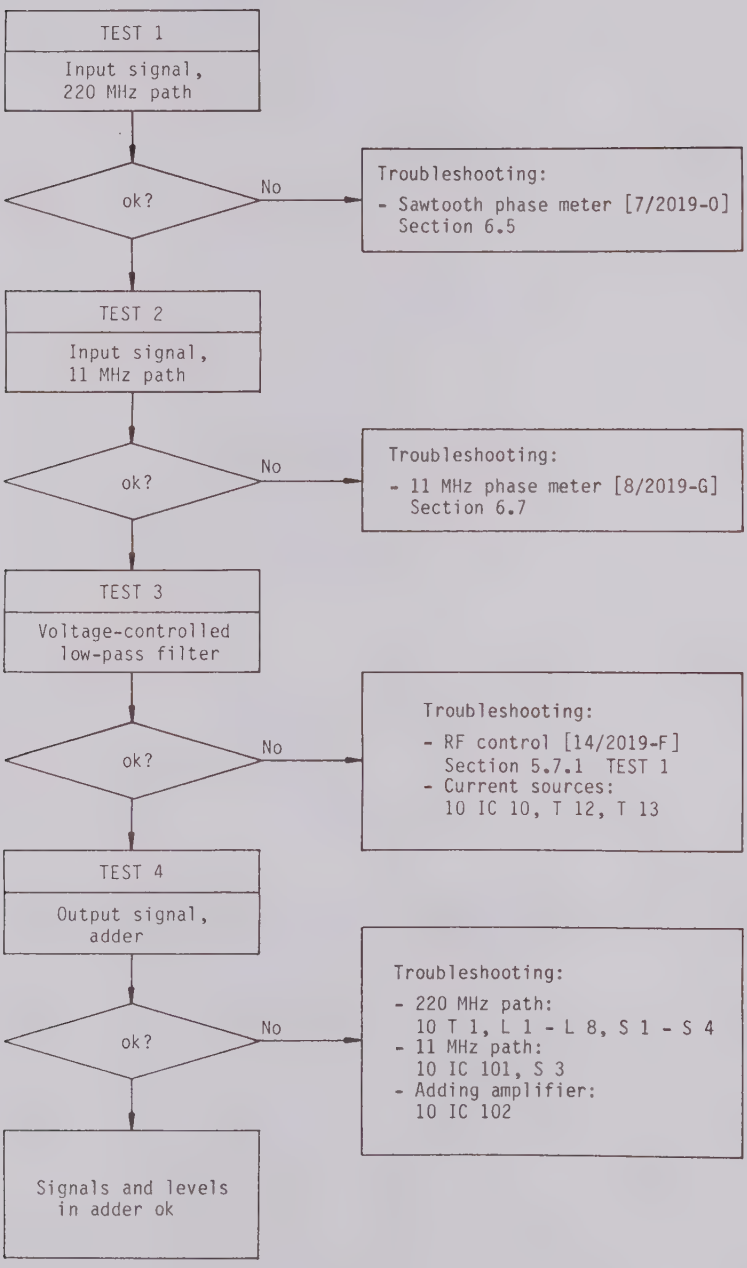
Further fault localization:



Note: The measurement in Section 4.7.1.2 involves certain difficulties, since only short-term inherent jitter measurements are possible as a result of the VCO drift.

5.6 ADDER [10/2019-AF] (F)

5.6.1 CONTROL OF SIGNALS AND CONTROL VOLTAGES



TEST 1: Input signal, 220 MHz path

Operate the PJM-4 with a clock signal from the PJG-4 (e.g. 34.368 Mbit/s)

Settings: - PJG-4: Jitter mod. 100 kHz, sine-wave, 0.5 UI
- PJM-4: Via "ENTW" test menu (see Section 9.3), set REGELGRENZFREQUENZ = 12 kHz

Check signal $U_{\varphi 2}$ at input 10 Pt. 4 using an oscilloscope:

$$U_{\varphi 2} = 300 \ldots 400\ mV_{pp}$$

TEST 2: Input signal, 11 MHz path

Operate the PJM-4 with a clock signal from the PJG-4 (e.g. 34.368 Mbit/s)

Settings: - PJG-4: Jitter mod. 1 kHz, sine-wave, 1 UI
- PJM-4: Via "ENTW" test menu, set "TEST AUS"

Check signal $U_{\varphi 1}$ at input 10 Pt. 9 using an oscilloscope:

$$U_{\varphi 1} = 120 \ldots 160\ mV_{pp}$$

TEST 3: Voltage-controlled low-pass filter

Operate the PJM-4 without an input signal

Select the built-in bit rates consecutively.

Use a DVM to measure: - The control voltage U_{LP} at 10 Pt. 2
- The current source setting via 10 R 18 and/or R 19

Bit rate/Mbit set	I/mA	U/mV via R 18/19	U_{LP}/V 10 Pt. 2
0.704	0.00289	2.89	0.033
2.048	0.00833	8.33	0.096
8.448	0.0345	34.5	0.40
25.776	0.105	105	1.21
34.368	0.140	140	1.61
139.264	0.568	568	6.53
167.117	0.681	681	7.84

Here: I/mA = 0.0001699 x fBit/MHz

Permissible tolerance: $\pm$ 5 % absolute
$\pm$ 1 % relative

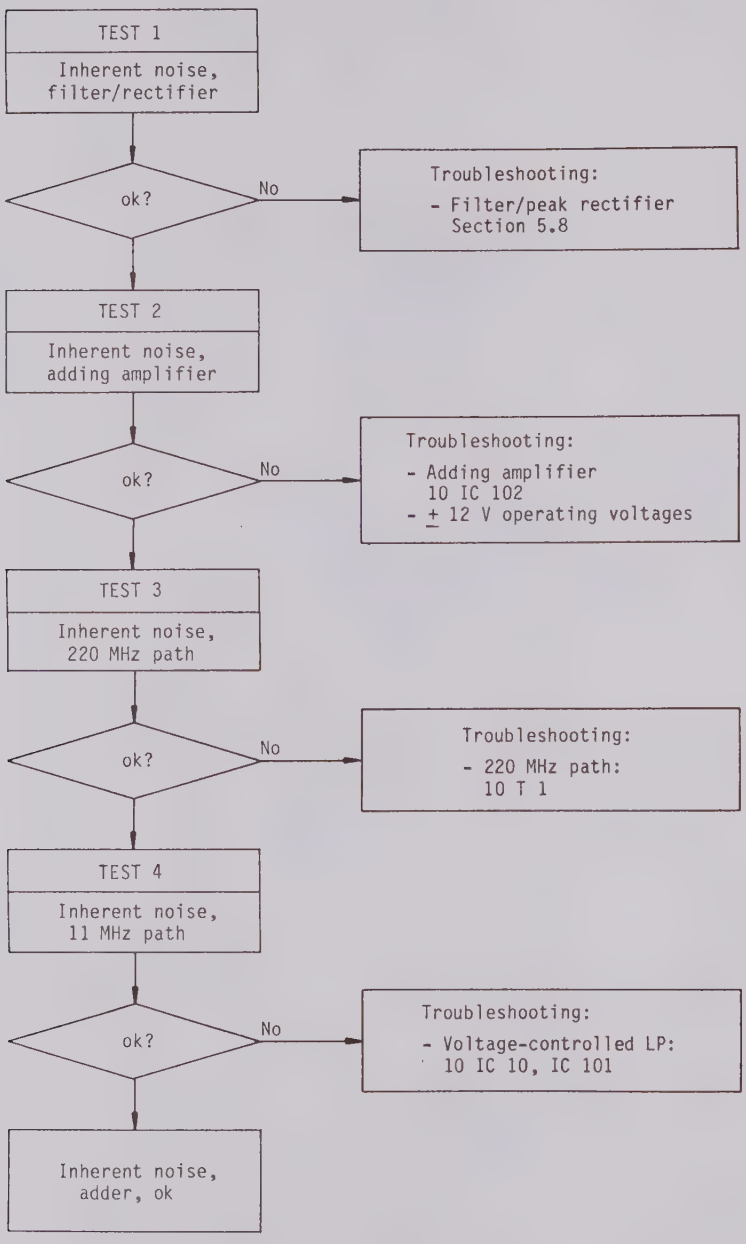
TEST 4: Output signal, adder

Settings as for TEST 2

Check the signal U_{JITTER} at output 10 Pt. 13 using an oscilloscope:

$$U_{JITTER} = \text{Approx. } 700\ mV_{pp}$$

5.6.2 TROUBLESHOOTING IN THE EVENT OF EXCESSIVE BASIC NOISE



TEST 1: Inherent noise, filter/peak rectifier

Operate the PJM-4 with a 34.368 Mbit/s clock signal from the PJG-4.

Remove the adder and connect 10 Pin 13 in the trough to ground.

Compare the displayed value with Table 5.6.2-1.

Re-install the adder.

TEST 2: Inherent noise, adding amplifier

Operate the PJM-4 without an input signal.

In the adder: Open switch 10 S 4 (220 MHz path OFF)
Flip switch 10 S 3 (11 MHz path OFF)

Via the "ENTW" test menu (see Section 9.3), set the following:
in the "EING-STUFE" menu: - EINGANGSTEILER = 20 dB
in the "RAST-EINST" menu: - REGLER 1 "KLEMM"
- RASTHILFE "EIN"
Press the RETURN key to return to the measuring program.

Compare the displayed value with Table 5.6.2-1.

TEST 3: Inherent noise, 220 MHz path

Operate the PJM-4 without an input signal.

In the adder: Close switch 10 S 4 (220 MHz path ON)
Flip switch 10 S 3 (11 MHz path OFF)

Via the "ENTW" test menu (see Section 9.3), set the following:
Same as for TEST 2

Compare the displayed value with Table 5.6.2-1.

TEST 4: Inherent noise, 11 MHz path

Operate the PJM-4 without an input signal.

Remove controller 1 [2019-H] and connect 9 Pin 6 in the trough to ground.
In the adder: Open switch 10 S 4 (220 MHz path OFF)
Flip switch 10 S 3 into normal position (11 MHz path ON)

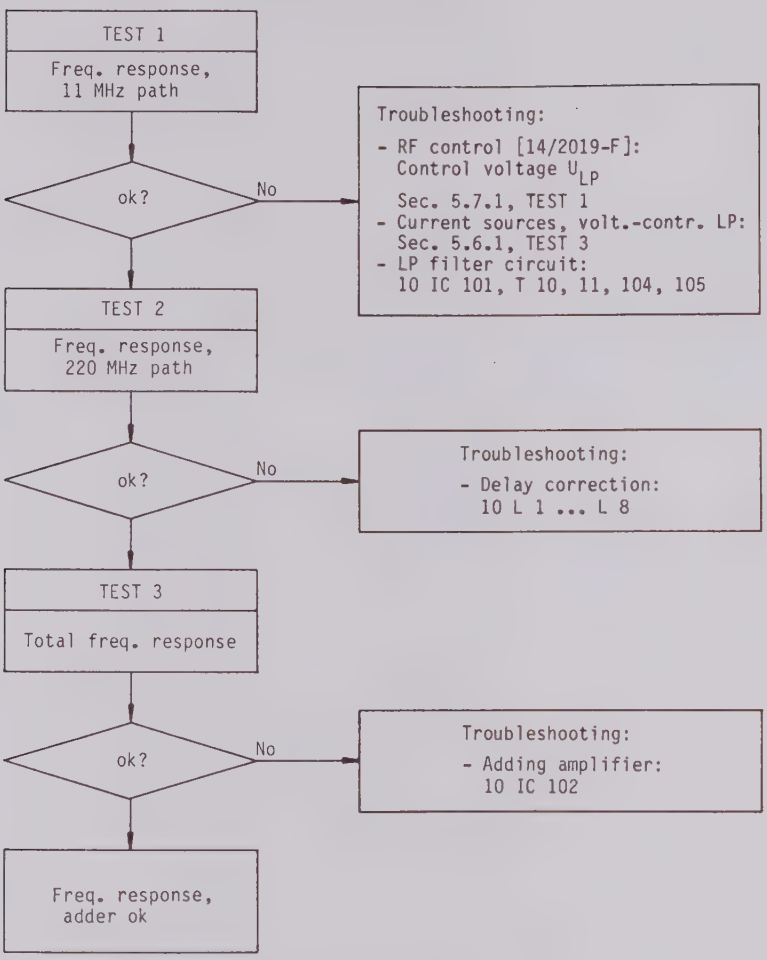
Via the "ENTW" test menu (see Section 9.3), set the following:
Same as for TEST 2

Compare the displayed value with Table 5.6.2-1.
Displayed values with testprogram BASIC NOISE (see section 4.5.3.1).

Set bandwidth	Displayed values			
	TEST 1	TEST 2	TEST 3	TEST 4
2 Hz - 600 kHz	< 3 mUI	< 3 mUI	< 3 mUI	< 3 mUI
2 Hz - 6700 kHz	< 4 mUI	< 8 mUI	< 8 mUI	< 8 mUI

Fig. 5.6.2-1 Table

5.6.3 FREQUENCY RESPONSE CHECK



TEST 1: Frequency response, 11 MHz path

Operate the PJM-4 without an input signal. Use SNA-1 and TK-11 to perform the measurement.

Settings: PJM-4: - Call up testprogram BASIC NOISE (see section 4.5.3.1)
- 139.368 Mbit/s
- Remove Controller 1 [9/2019-H] and feed with SNA-1 generator at 9 Pin 6 in the trough: -15 dBm
- Use the "ENTW" test menu (see Section 9.3) to set the following:
in the "EING-STUFE" menu:
Input divider = 20 dB
in the "RAST-EINST" menu:
Controller 1 "KLEMM"
Lock-in aid "EIN"

SNA-1: - NETWORK ANALYSIS:
FSTART = 1 kHz, 3 decades
REFERENCE = -23 dBm, SCALE = 1 dB
RWB = 300 Hz, VBW = 5 kHz, SWT = 2 s
SEND LEVEL = -15 dBm
Normalize: Measure with the TK-11 at the generator input point and normalize the SNA-1

Use the active test probe TK-11 to measure at 10 IC 101, Pin 6:
Max. deviation up to 1 MHz (referred to 1 kHz): $\pm$ 0.2 dB

TEST 2: Frequency response, 220 MHz path

Test setup and settings as per alignment instructions in Section 7.2.6.1

Deviations: PJG-4: - 139.264 Mbit/s

PJM-4: - 139.264 Mbit/s, clock
- Use the "ENTW" test menu (see Section 9.3) to set the following:
Control limit frequency = 2 kHz

SNA-1: - Measurements and normalization with TK-11

At adder input 10 Pt. 4, use the TK-11 to store the reference curve in <M> and compare it with the signal at Pt. 10 L 8, C 15, C 18 <A & M>:
Max. deviation up to 3 MHz (referred to 4 kHz): $\pm$ 0.2 dB

TEST 3: Total frequency response

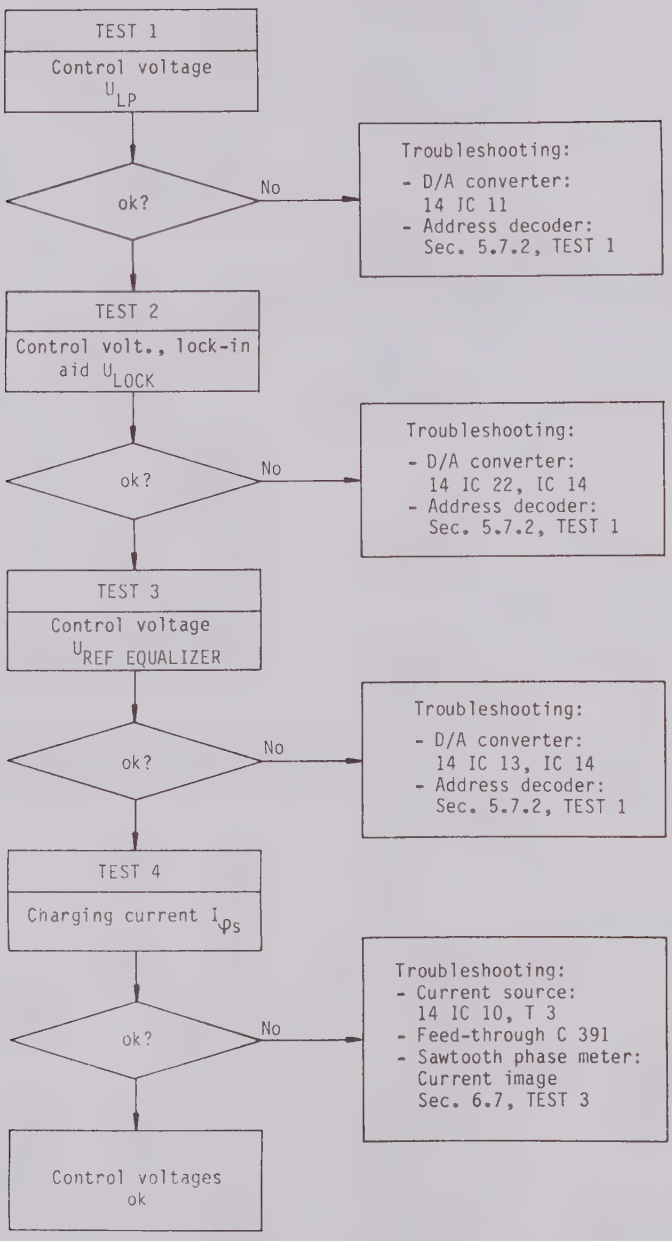
Test setup and settings as for TEST 2

At adder input 10 Pt. 4, use the TK-11 to store the reference curve in <M> and compare it with the signal at adder output 10 Pt. 13 <A & M>:

Max. deviation, referred to 4 kHz: up to 3 MHz $\pm$ 0.2 dB
up to 4 MHz $\pm$ 0.3 dB

5.7 RF CONTROL [14/2019-AF] (G)

5.7.1 CHECKING CONTROL VOLTAGE GENERATION



TEST 1: Control voltage U_{LP}

Operate the PJM-4 without an input signal.

Via the "SERVICE" test menu (see Section 9.3), call up the associated cyclic hardware test program (9.3.5) in the monitor program (9.3.4):

"S : 1 1 9 H"

Use the oscilloscope at 10 Pt. 2 in the adder [2019-AF] (due to better accessibility) to measure the sawtooth oscillation:

U_{min} = 0 V
U_{max} = Approx. 8 V

TEST 2: Control voltage, lock-in aid U_{LOCK}

Operate the PJM-4 without an input signal.

Via the "SERVICE" test menu (see Section 9.3), call up the associated cyclic hardware test program (9.3.5) in the monitor program (9.3.4):

"S : 1 1 F H"

Use the oscilloscope at 9 Pt. 8 in Controller 1 [2019-H] (due to better accessibility) to measure the sawtooth oscillation:

U_{min} = -7 V
U_{max} = +7 V

TEST 3: Control voltage $U_{REF\ EQUALIZER}$

Operate the PJM-4 without an input signal.

Via the "SERVICE" test menu (see Section 9.3), call up the associated cyclic hardware test program (9.3.5) in the monitor program (9.3.4):

"S : 1 2 5 H"

Use the oscilloscope at 2 Pt. 22 in input circuit [2019-V] (due to better accessibility) to measure the sawtooth oscillation:

U_{max} = 0 V
U_{min} = -2 V

TEST 4: Current source for sawtooth phase meter

Via the "ENTW" test menu, set the following in the "REGELKREISE" menu:
Current source = 5.6 mA

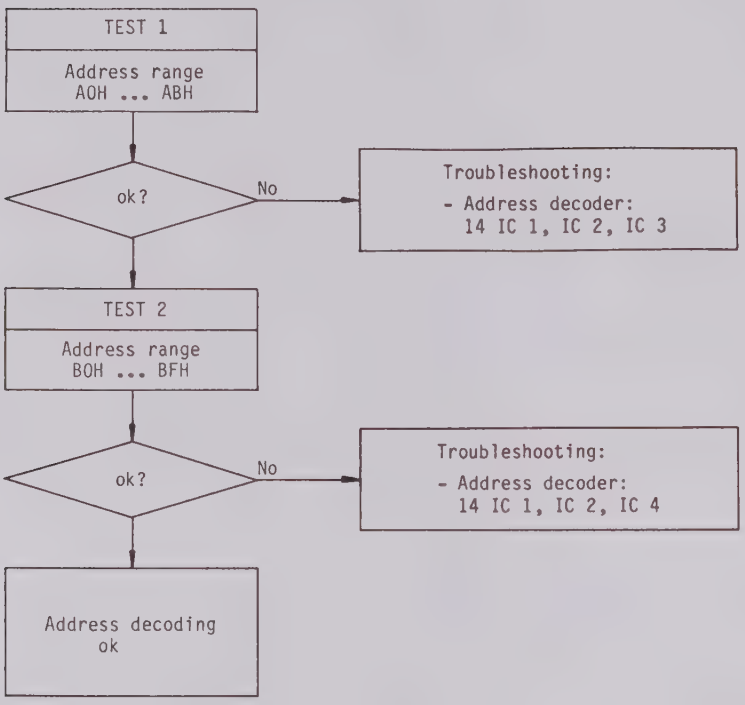
1. Use a DVM to measure at 14 IC 10, Pin 2 (virtual zero point):

U = 0 V

2. Connect the DVM to output 14 Pt. 32:

$U \leq -2.5$ V

5.7.2 FAULTY ADDRESS DECODING



TEST 1: Address range AOH ... ABH

Operate the PJM-4 without an input signal.

Via the "SERVICE" test menu (see Section 9.3), call up the associated cyclic hardware test program (9.3.5) in the monitor program (9.3.4):

"S : 1 0 D H"

Use an oscilloscope to measure the address pulses at the decoder outputs of 14 IC 2/2 and IC 3:

Period : Approx. 3.5 kHz
"LOW" pulse duration: Approx. 2.2 µs

TEST 2: Adress range BOH ... ABH

Operate the PJM-4 without an input signal.

Call up the cyclic hardware test program (see TEST 1):

"S : 1 1 3 H"

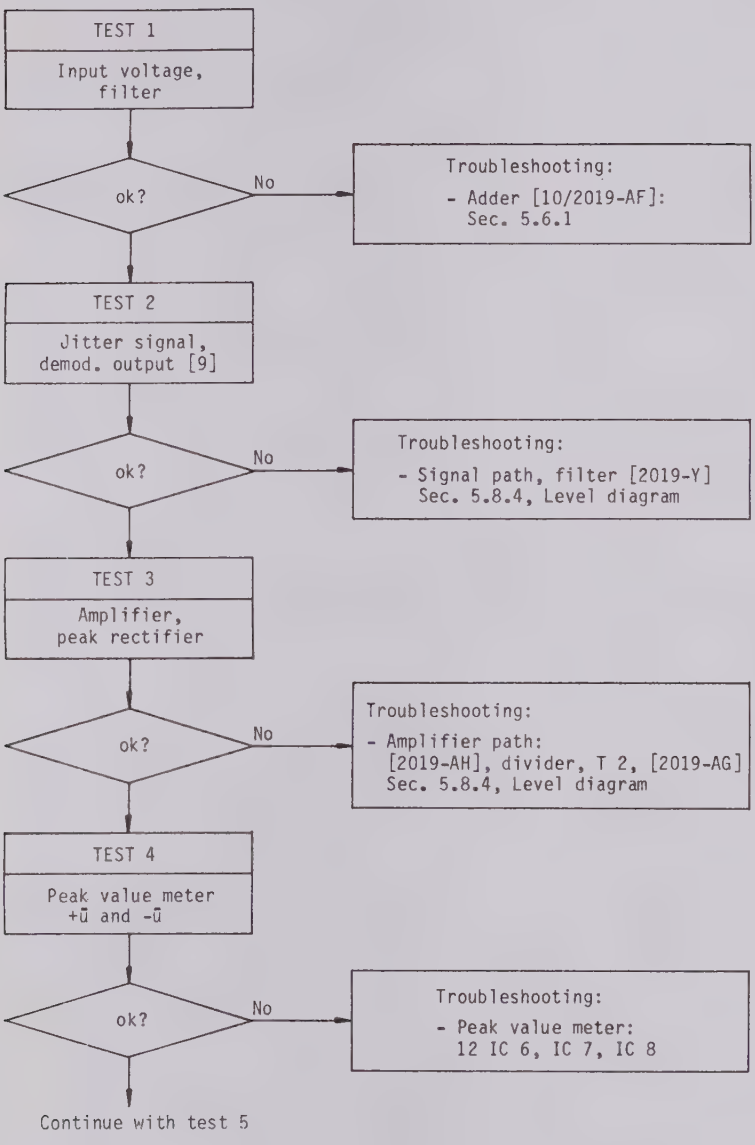
Use an oscilloscope to measure the address pulses at outputs 14 IC 4:

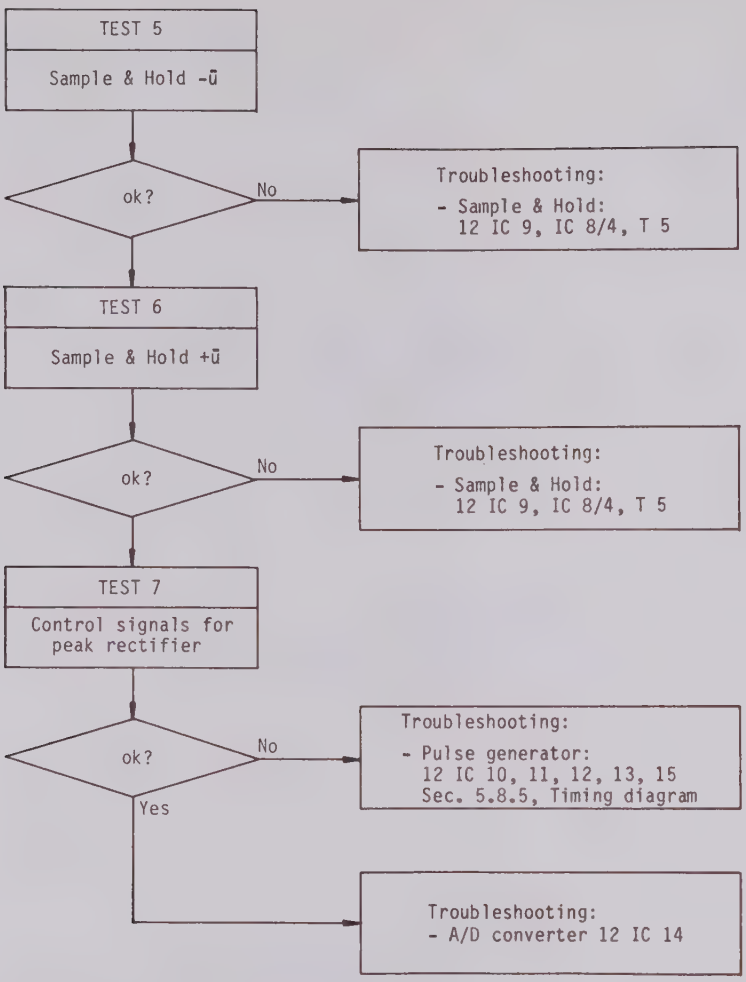
IC 4, Pin 8 Address range BOH ... B7H
IC 4, Pin 6 Address range B8H ... BFH

Period : Approx. 46 kHz
"LOW" pulse duration: Approx. 2.2 µs

5.8 FILTER/RECTIFIER [11/2019-Y/Z] (H/K)

5.8.1 FAULTY JITTER DISPLAY





Test setup for troubleshooting in the jitter evaluation circuit (filter/rectifier)

Instruments required:	1 jitter generator	PJG-4	W&G
	1 oscilloscope BW > 20 MHz		
	1 DVM	8050 A, 8600 A	Fluke

Test setup: Connect clock output [22], PJG-4, to input [8], PJM-4.

Settings:

- PJG-4: 8448 kbit/s, clock
  Modulation: Sinusoidal
  Jitter: 1 UI, 1 kHz
- PJM-4: 8448 kbit/s, clock
  Code: NRZ/ECL
  High-pass: 2 Hz
  Low-pass: 300 kHz

TEST 1: Input voltage, filter

Use an oscilloscope to measure the input voltage of the filter card at 11 Pt. 12 c:
Required: U = 700 mV_{pp}

TEST 2: Jitter signal, demod. output

Use an oscilloscope to measure the jitter signal at demod. output [9] with high impedance:
Required: U = 220 mV_{pp}

TEST 3: Amplifier, peak rectifier

On the PJG-4, set the jitter span in such a way as to obtain 247.5 mV_{rms} at the filter card input 11 Pt. 12 c, measured with a Fluke 8050 A or 8600 A DVM.

Use an oscilloscope and test probe (short ground connection!) to measure the jitter signal at 12 TP 1 on the rectifier card:
Required: AC U = 3.5 V_{pp}
DC U $\leq$ 20 mV

TEST 4: Peak value meter for $+\bar{u}$ and $-\bar{u}$

Use an oscilloscope to measure the peak jitter values at 12 IC 8/1, Pin 14, and 12 IC 8/2, Pin 8 on the rectifier card:
Required: IC 8/1, Pin 14 : $-\hat{U}$ = -1.75 V $\pm$ 100 mV
IC 8/2, Pin 8 : $+\hat{U}$ = -1.75 V $\pm$ 100 mV

TEST 5: Sample & Hold $-\bar{u}$

On the rectifier card, connect 12 Pt. e 8 or 12 IC 9/1, Pin 9, to ground.

At 12 Pt. e 4 or 12 IC 14, Pin 35, measure with a Fluke 8050 or 8600 DVM at high impedance:
Required: U = +2.1 V

TEST 6: Sample & Hold $+\bar{u}$

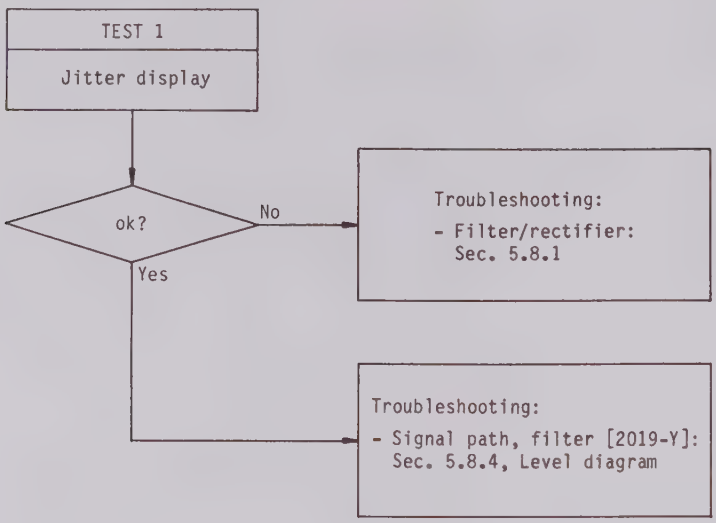
On the rectifier card, connect 12 Pt. e 8 to +5 V.

Repeat the measurement in TEST 5:
Required: U = +2.1 V

TEST 7: Control signals for peak rectifier

Check the digital signals as per timing diagram 5.8.5.

5.8.2 FAULTY DEMOD. SIGNAL

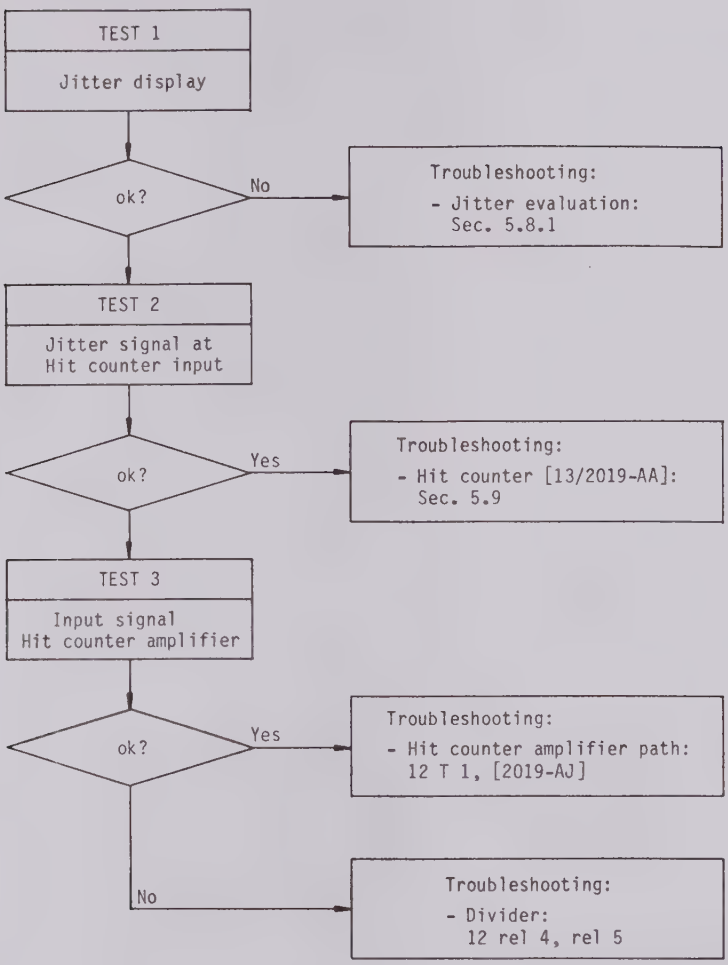


TEST 1: Jitter display

Test setup and settings as per Section 5.8.1.

Required display: 1 UI_{pp} + inherent noise (approx. 5 mUI_{pp})

5.8.3 FAULTY HIT COUNTER DISPLAY



TEST 1: Jitter display

Test setup and settings as per Section 5.8.1

Required display: 1 UI_{pp}

TEST 2: Jitter signal at hit counter input

Test setup and settings as per Section 5.8.1

On the PJM-4, set: - Phase hits ON
- Threshold 0.4 UI_p

Use an oscilloscope to measure the hit counter signal at 11 Pt. 5 on the filter card:
Required: 4 V_{pp}

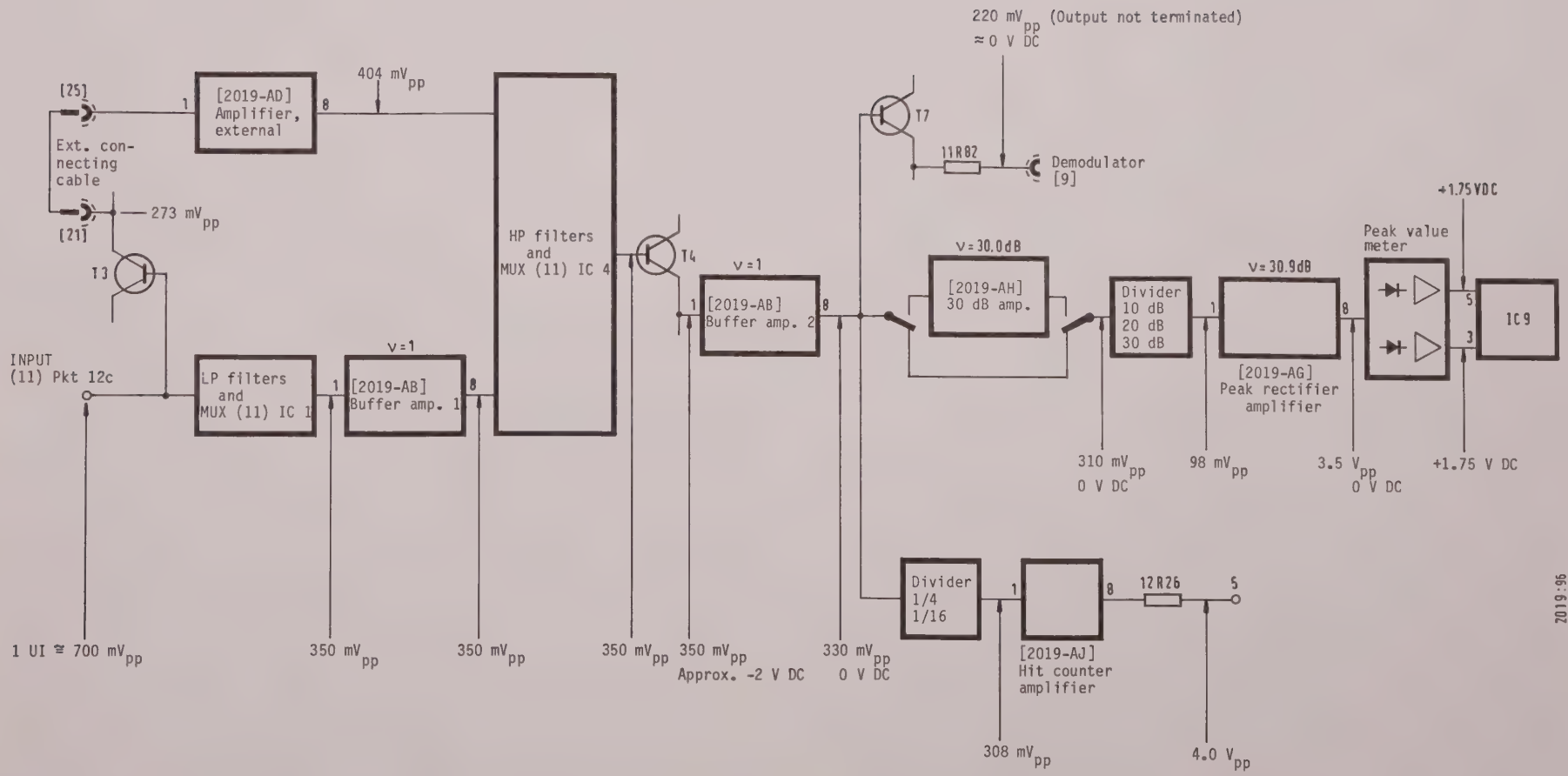
TEST 3: Input signal, hit counter amplifier

Test setup and settings as for TEST 2.

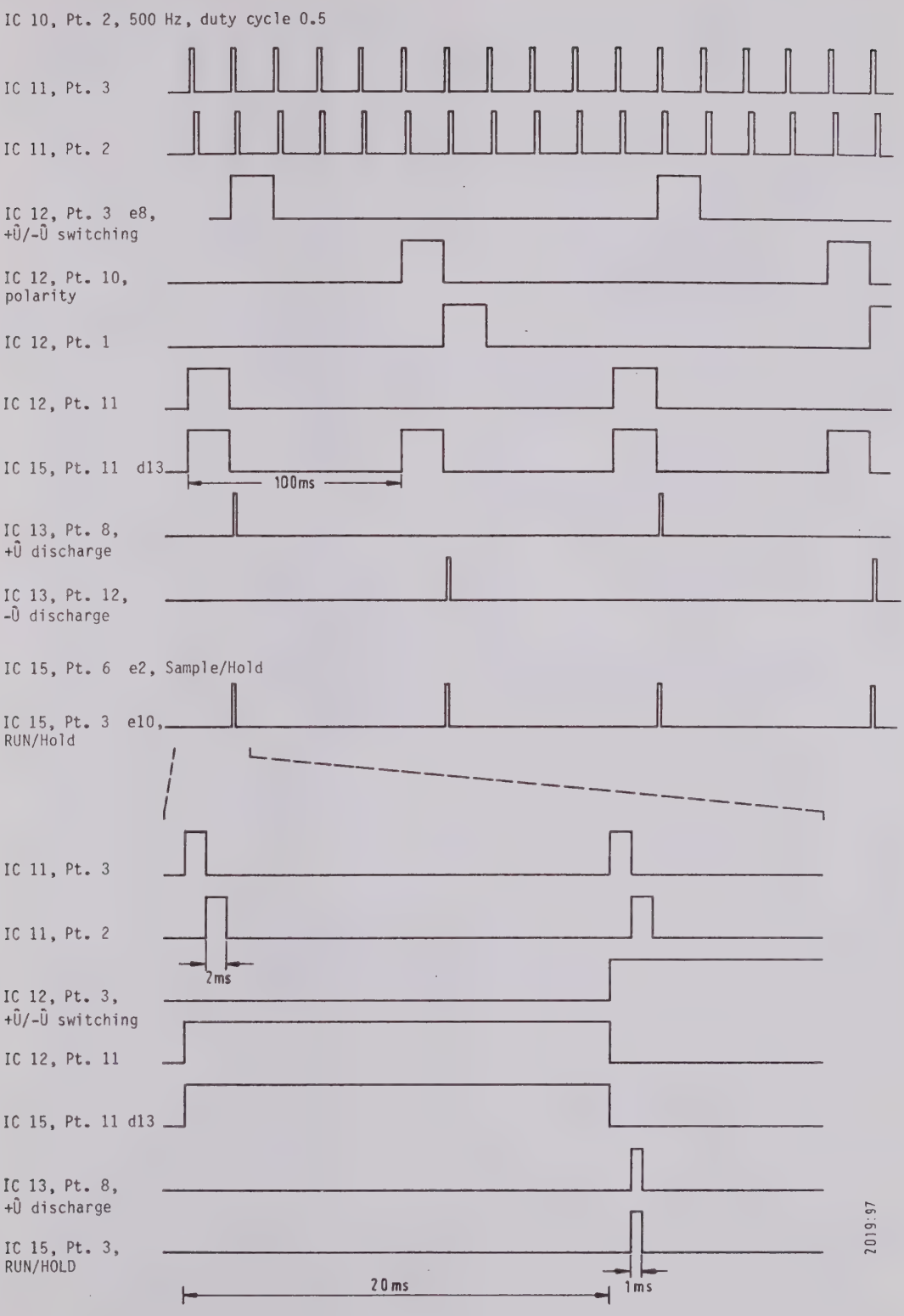
Use the oscilloscope to measure the voltage at 12 rel 4, Pin 4, on the rectifier card:
Required: 308 mV_{pp}

5.8.4 LEVEL DIAGRAM, FILTER (11) AND PEAK RECTIFIER (12)

Instrument settings and test setup as per Section 5.8.1
GAIN CORR [23] right-hand stop, THRSH 0.4 UI_p

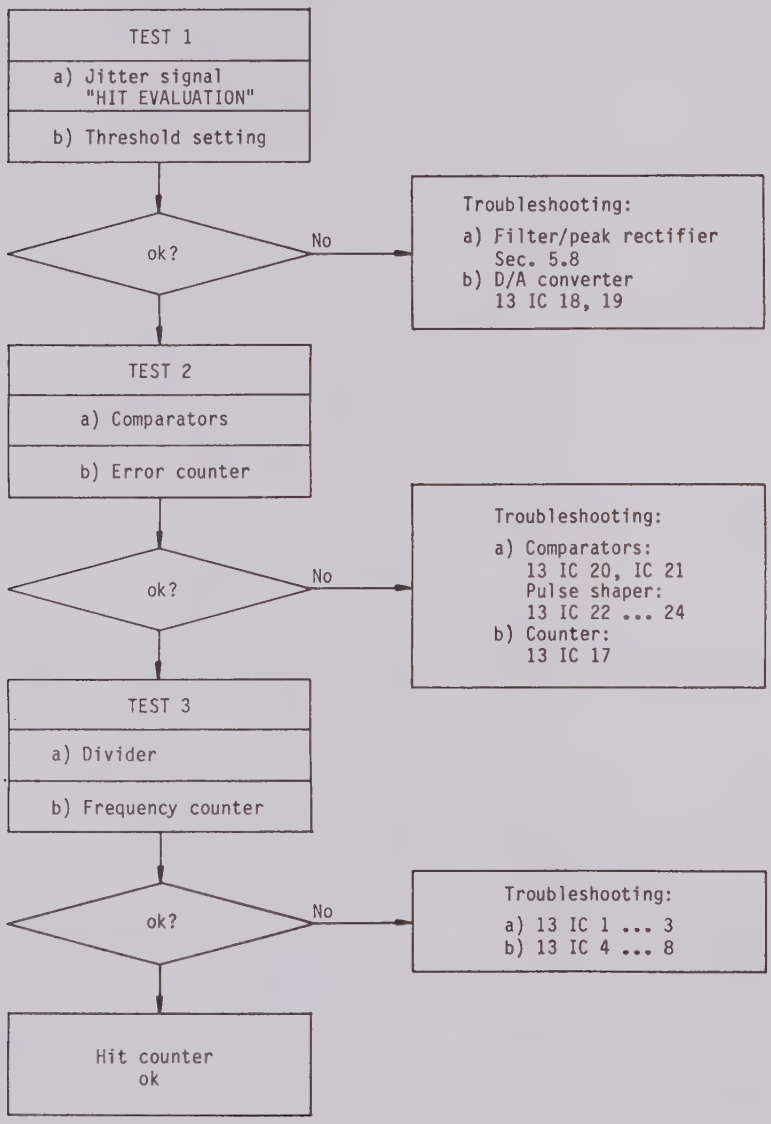


5.8.5 TIMING DIAGRAM, PEAK RECTIFIER



5.9 HIT COUNTER [13/2019-AA] (I)

5.9.1 FUNCTIONAL CHECK



TEST 1: Jitter signal and threshold setting

Feed the PJM-4 with a clock signal from the PJG-4.

Settings: PJG-4: - 34.368 Mbit/s, clock signal
- Sinusoidal modulation ON: 1 kHz, 2 UI_{pp}
PJM-4: - 34.368 Mbit/s, clock

Use an oscilloscope to check the jitter signal at 13 TP 10 and a DVM to check the threshold voltages at 13 TP 8 and TP 9:
The values are as follows for the THRESHOLD settings listed below:

	TEST 1a	TEST 1b
THRESHOLD setting	TP 10	TP 8, TP 9
0.5 UI	8 V_{pp}	Approx. 2 V
1 UI	2 V_{pp}	Approx. 1 V
6 UI	0.5 V_{pp}	Approx. 1.5 V

TEST 2: Comparators and error counter

Feed the PJM-4 with a clock signal from the PJG-4.

Settings: As for TEST 1

TEST 2a: Use an oscilloscope (BW > 100 MHz) to check the pulses at TP 13 and TP 14:
f = 1 kHz T_i = Approx. 50 ns

TEST 2b: Start hit counting on the PJM-4: GATING = 1 s, THRESHOLD = 0.5 UI
PHASEHITS displayed: Approx. 2000

TEST 3: Divider and frequency counter

Feed the PJM-4 with a clock signal from the PJG-4.

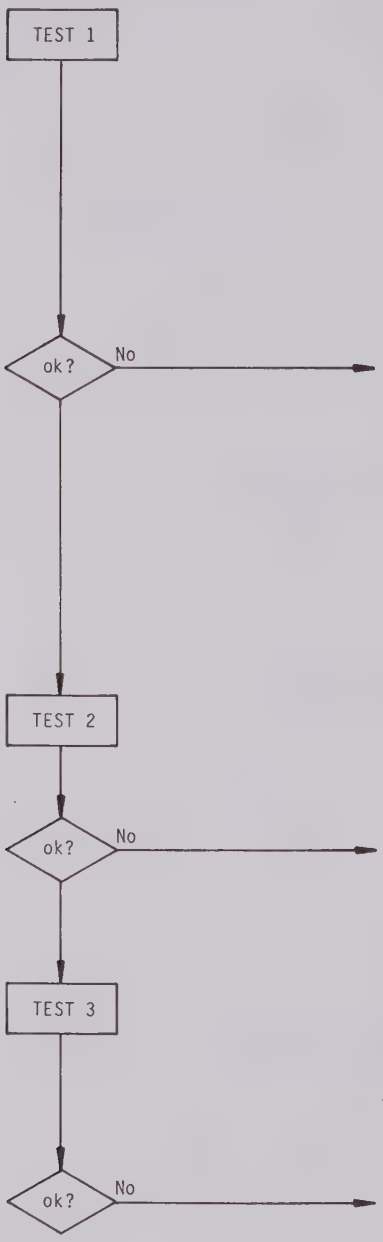
Settings: As for TEST 1

TEST 3a: Check the divided clock frequency at 13 TP 3:
f = Bit rate frequency/10 (here: 3.4368 MHz)

TEST 3b: Use the "ENTW" test menu to read out the frequency counter:
Regenerated clock = Bit rate frequency

5.10 DISPLAY/CONTROL SECTION (L)

5.10.1 FUNCTIONAL CHECK



Use the "SERVICE" test menu (see Section 9.3) to call up the keyboard hardware test program (9.3.5) in the monitor program (9.3.4):
"S: 13D "

If this is impossible due to a faulty keyboard, call up via: - MONEX control section "S: 13D"
- IEC bus "S: 013D,"
- DIP switch on CPU-2A (9.3.5)

The designation of the key pressed in each case is displayed.

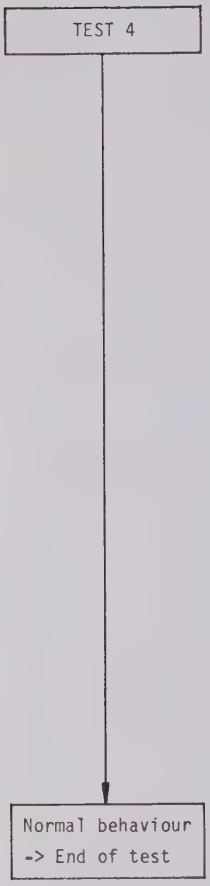
Troubleshooting:
- 1 key is displayed constantly: Key sticking
  Short-circuit
- Keys are not displayed : Key does not close
  Line interruption,
  IC 5, IC 6
  I/O bus: Data
- No key is displayed : +5 V operating voltage
  Connector, cable
  IC 5, IC 6

Test control in normal operation

Troubleshooting:
- Keyboard debouncing IC 8 ... IC 11
- I/O bus: Data, addresses
- CPU (booting)

Use the "SERVICE" test menu (see Section 9.3) to call up the cyclic LED test program (9.3.5) in the monitor program (9.3.4):
"S: 137"
LEDs light up in the specified order/high-low beep tone

Troubleshooting:
- Individual LEDs off: LED faulty
  Driver, keyboard IC 4, IC 5
  Display IC 4, IC 5, IC 6
  Address decoder
  I/O bus: Data
- All LEDs OFF: For keys, +5 V operating voltage
  For display, +5 V/-12 V operating voltage
  I/O bus, connector, cable



Display behaviour

- Display fully dark -> Troubleshooting in voltage generator
  -> Troubleshooting in computer core
  -> Troubleshooting in command transfer
  -> Troubleshooting in data transfer
- Single digits missing -> Troubleshooting in multiplexer/column driver
- Single pixels missing in all digits
  -> Troubleshooting in character generator/anode driver
- Cursor missing -> Troubleshooting in cursor driver
- Display Error 511 -> Troubleshooting in command transfer
- Display Error 512 -> Troubleshooting in data transfer
- Display Error 500 -> Troubleshooting in computer RAM/EPROM
- Single pixels very bright, meaningless pattern
  -> Troubleshooting in multiplexer
  -> Troubleshooting in computer core

  CAUTION: Disconnect +12 V operating voltage (e.g. at L 1), to avoid damage!
- Other abnormal behaviour

  Troubleshooting: Switch S 1 open, S 2 in normal setting/ operating voltages/multiplexer/character generator

  Command: Transfer/data transfer/I/O bus/CPU

5.10.2 TROUBLESHOOTING

5.10.2.1 Troubleshooting in voltage generator

TEST 1

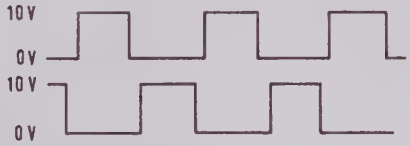
Measure +12 V operating voltage at L 1

ok? — No → Troubleshooting: - Connector
- Cable
- Power supply unit

TEST 2

Measure clock signal at IC 1, Pin 11/14

U = 10 V_{pp}, f ≈ 130 Hz, 3 µsec HIGH, not overlapping



ok? — No → Troubleshooting: - 16 IC 1

TEST 3

Primary side voltage O 1 connection (1)/(8)

U = 10 V_{pp}, f ≈ 130 Hz

ok? — No → Troubleshooting: - Primary circuit
16 T 1, T 4, O 1, C 1

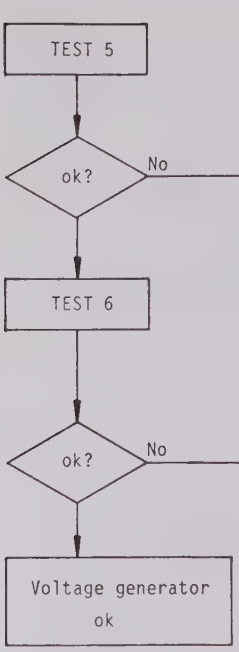
TEST 4

Secondary side voltage O 1 connection (3)/(6)

U ≈ 80 V_{pp}, f ≈ 130 Hz

ok? — No → Troubleshooting: - Secondary circuit
16 O 1, Gl 3, Gl 4, C 8

Common fault: Winding connection in O 1 or
short to pot core (≅ ground)



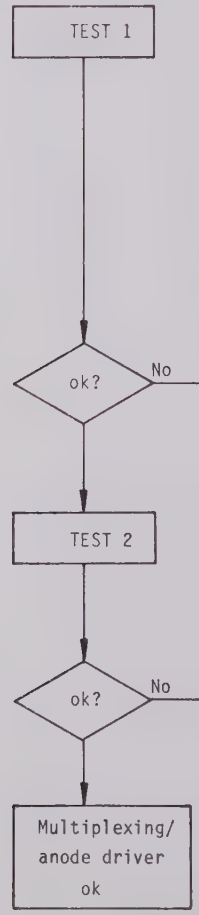
Measure 40 V voltage
U = 35 $V_{=}$ ... 40 $V_{=}$, depending on load imposed by illuminated display elements

Troubleshooting: - 16 IC 8, IC 19 ... IC 25, Rö 1

Secondary side voltage O 1 connection (9)/(12)
U ≈ 8 V_{pp} + 9 $V_{=}$

Troubleshooting: - Secondary circuit:
16 O 1, Gl 2, Rö 1

5.10.2.2 Troubleshooting in multiplexer/column driver



Display Clock IC 19, Pin 21, and IC 25, Pin 7
Clock pulse period: 345 µsec, LOW duration: 5 µsec

Display Data IC 19, Pin 39, and IC 25, Pin 5
Multiplexer control period: 14 msec, HIGH duration: 125 µsec

Display Strobe IC 19, Pin 19, and IC 20-25, Pin 3
Strobe signal period: 345 µsec, HIGH duration: 50 µsec at maximum brightness

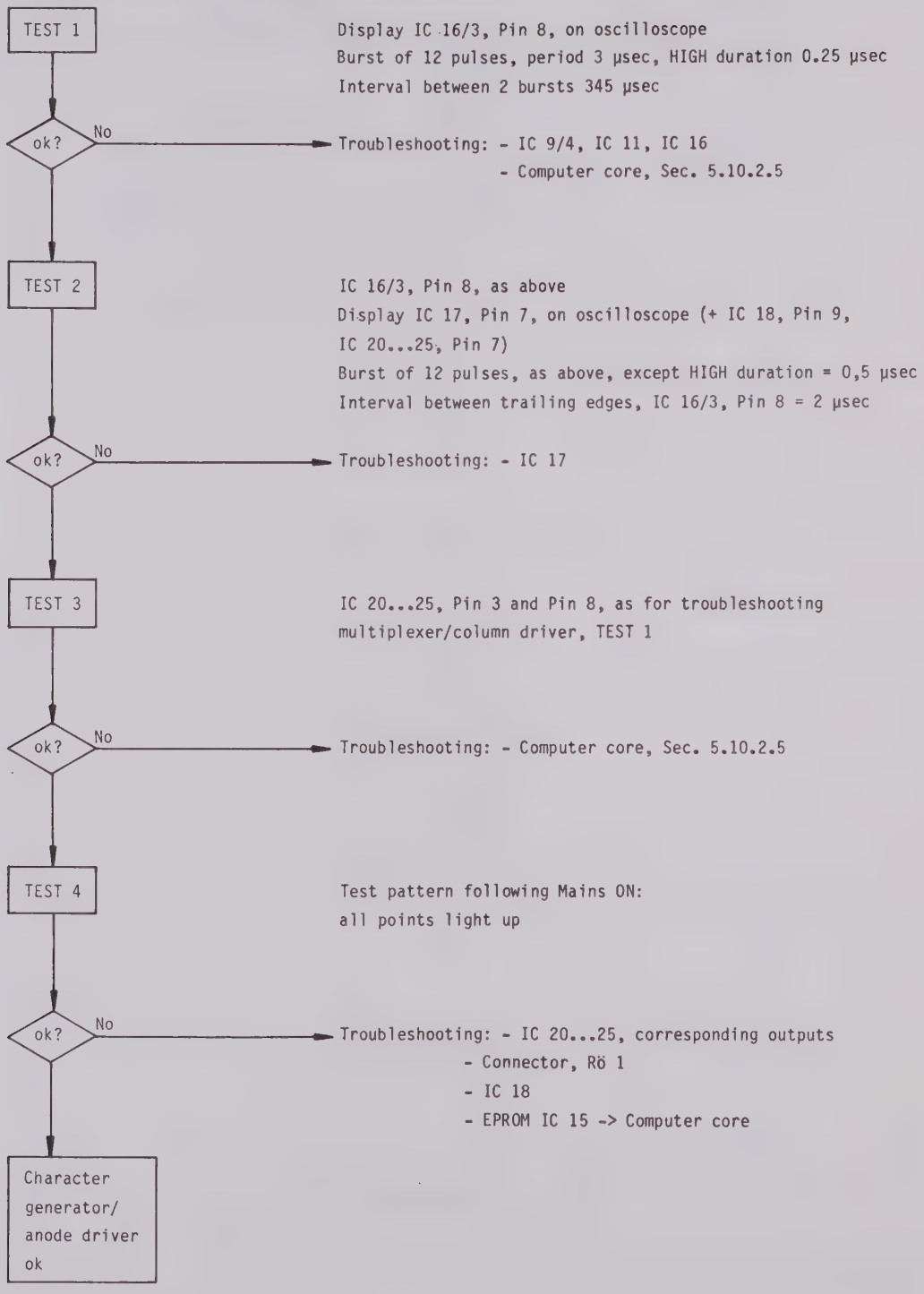
Display Latch Enable IC 19, Pin 22, and IC 20-25, Pin 8
LE signal period: 345 µsec, HIGH duration: 13 µsec

Troubleshooting: - Computer core, Sec. 5.10.2.5

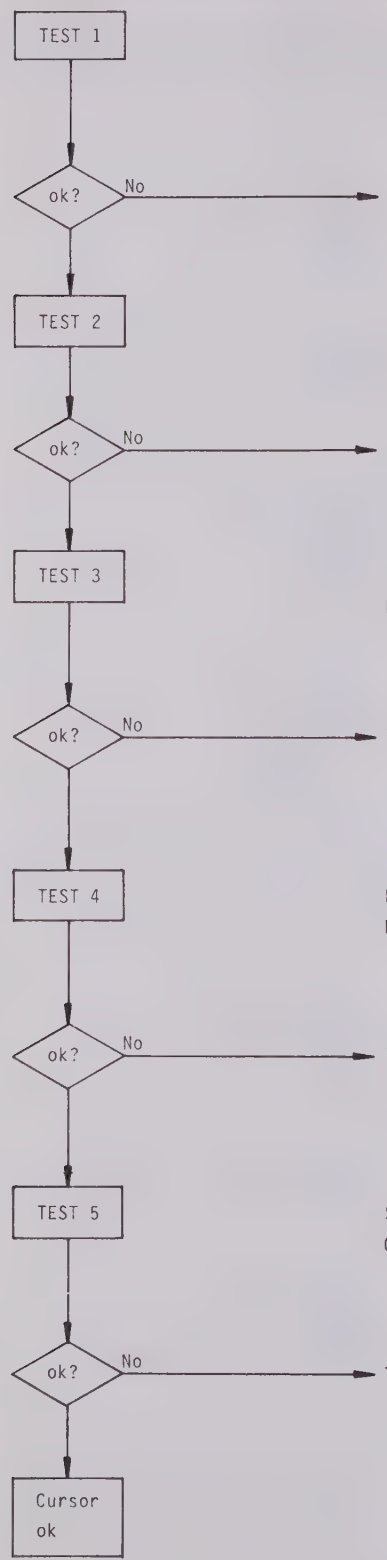
Test pattern after Mains ON, all columns light up

Troubleshooting: - Columns 1...8 IC 25
- Column 9...40 IC 19
- Connector
- Rö 1
- Voltage generator. Sec. 5.10.2.1

5.10.2.3 Troubleshooting in the character generator/anode driver



5.10.2.4 Troubleshooting in the cursor driver



In measuring menu, press SK 5 -> Menu page with 3 cursor ranges --> Cursors are set
Display IC 10/1, Pin 12, on oscilloscope
Pulse LOW duration 3.4 msec, HIGH duration 1.4 msec

Troubleshooting: - Computer core, Sec. 5.10.2.5

Display base of T 29 on oscilloscope
HIGH level 0.7 V LOW level < 0.7 V

Troubleshooting: - 16 IC 10/1, T 29

Display collector of T 29 on oscilloscope
HIGH level 40 V LOW level 0 V

Troubleshooting: - 16 T 29, T 30, Gl 5

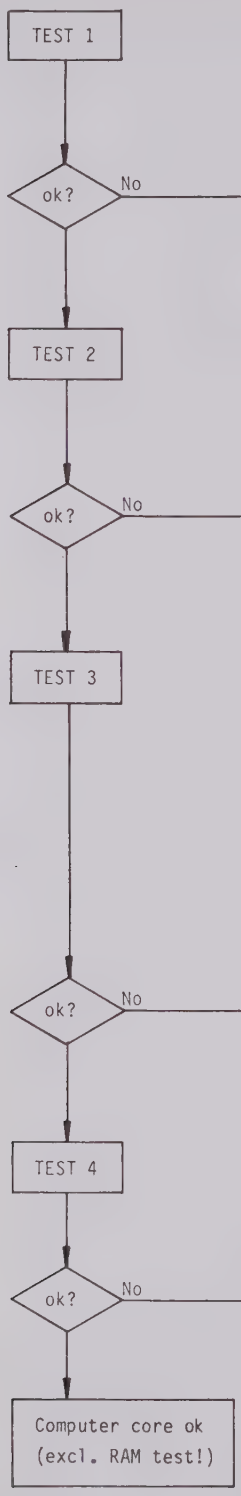
Display emitter of T 30 on oscilloscope
HIGH level 40 V LOW level 0 V

Troubleshooting: - 16 T 30, Gl 5

Service menu "S: 149"
Cursor display is switched on from right to left

Troubleshooting: - Multiplexer, Sec. 5.10.2.2
- Connector
- Rö 1

5.10.2.5 Troubleshooting in the computer core



Display system clock IC 12, Pin 18/19, on oscilloscope
$U = V_{pp}$, f = 12 MHz

Troubleshooting: - Crystal Q 1
- Operating voltage

Measure Reset input IC 12, Pin 9
$U \leq 0.8$ V · LOW level

Troubleshooting: - Connector, cable
- CPU-2A

Set free-running

S 2/1	OFF
S 2/2	ON
S 2/3	OFF
S 2/4	ON
S 2/5	OFF
S 2/6	ON

Display address signals at IC 13/IC 15 on oscilloscope
Square-wave signal AØ ... A7 with interference*, since address latch IC 14 transparent while ALE = HIGH; A8 ... A14 without interference

$f_{AØ}$ = 1 MHz f_{A14} = 61.03 Hz

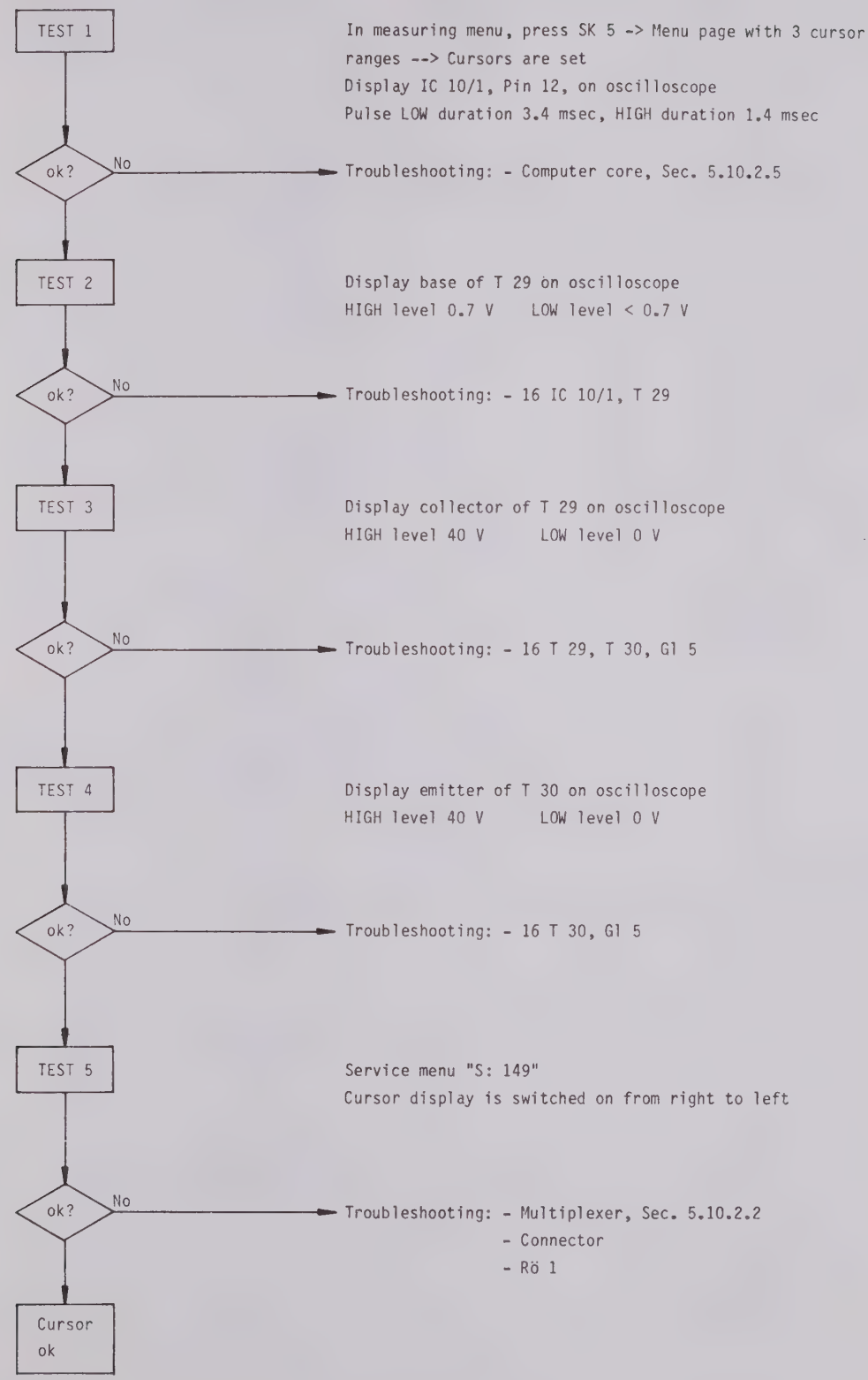
* Trigger with A8!

Troubleshooting: - Processor IC 12
- Address latch IC 14

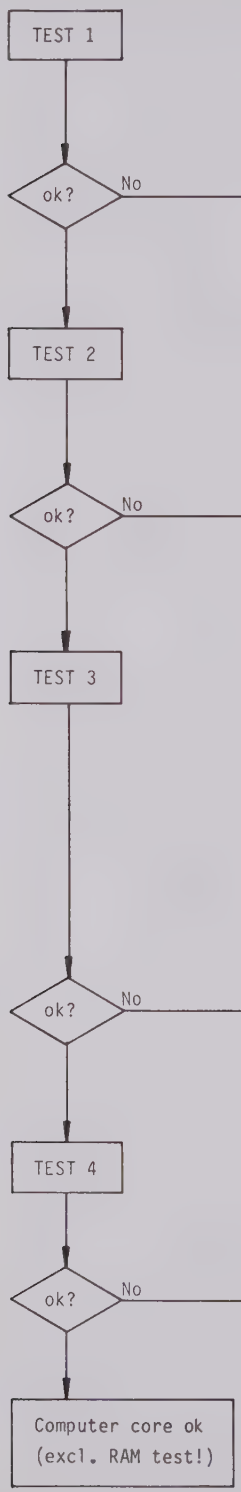
Record signature on EPROM with HP 5004 A signature analyzer

Troubleshooting: - EPROM IC 15
- Address latch IC 14

5.10.2.4 Troubleshooting in the cursor driver



5.10.2.5 Troubleshooting in the computer core



Display system clock IC 12, Pin 18/19, on oscilloscope
$U = V_{pp}$, f = 12 MHz

Troubleshooting: - Crystal Q 1
- Operating voltage

Measure Reset input IC 12, Pin 9
$U \leq 0.8$ V · LOW level

Troubleshooting: - Connector, cable
- CPU-2A

Set free-running
S 2/1 OFF
S 2/2 ON
S 2/3 OFF
S 2/4 ON
S 2/5 OFF
S 2/6 ON

Display address signals at IC 13/IC 15 on oscilloscope
Square-wave signal AØ ... A7 with interference*, since address latch IC 14 transparent while ALE = HIGH; A8 ... A14 without interference

$f_{AØ}$ = 1 MHz f_{A14} = 61.03 Hz

* Trigger with A8!

Troubleshooting: - Processor IC 12
- Address latch IC 14

Record signature on EPROM with HP 5004 A signature analyzer

Troubleshooting: - EPROM IC 15
- Address latch IC 14

Signature analysis for display processor 80C51

Check the signatures of EPROM IC 15

- Settings

  a) Signature analyzer HP 5004 A Start: ⌞
  Stop : ⌞
  Clock: ⌠

  b) Display control [2019-B], circuit diagram (16)

  Free-running switch S 2/1 OFF
  S 2/2 ON
  S 2/3 OFF
  S 2/4 ON
  S 2/5 OFF
  S 2/6 ON

- Signature analyzer connection

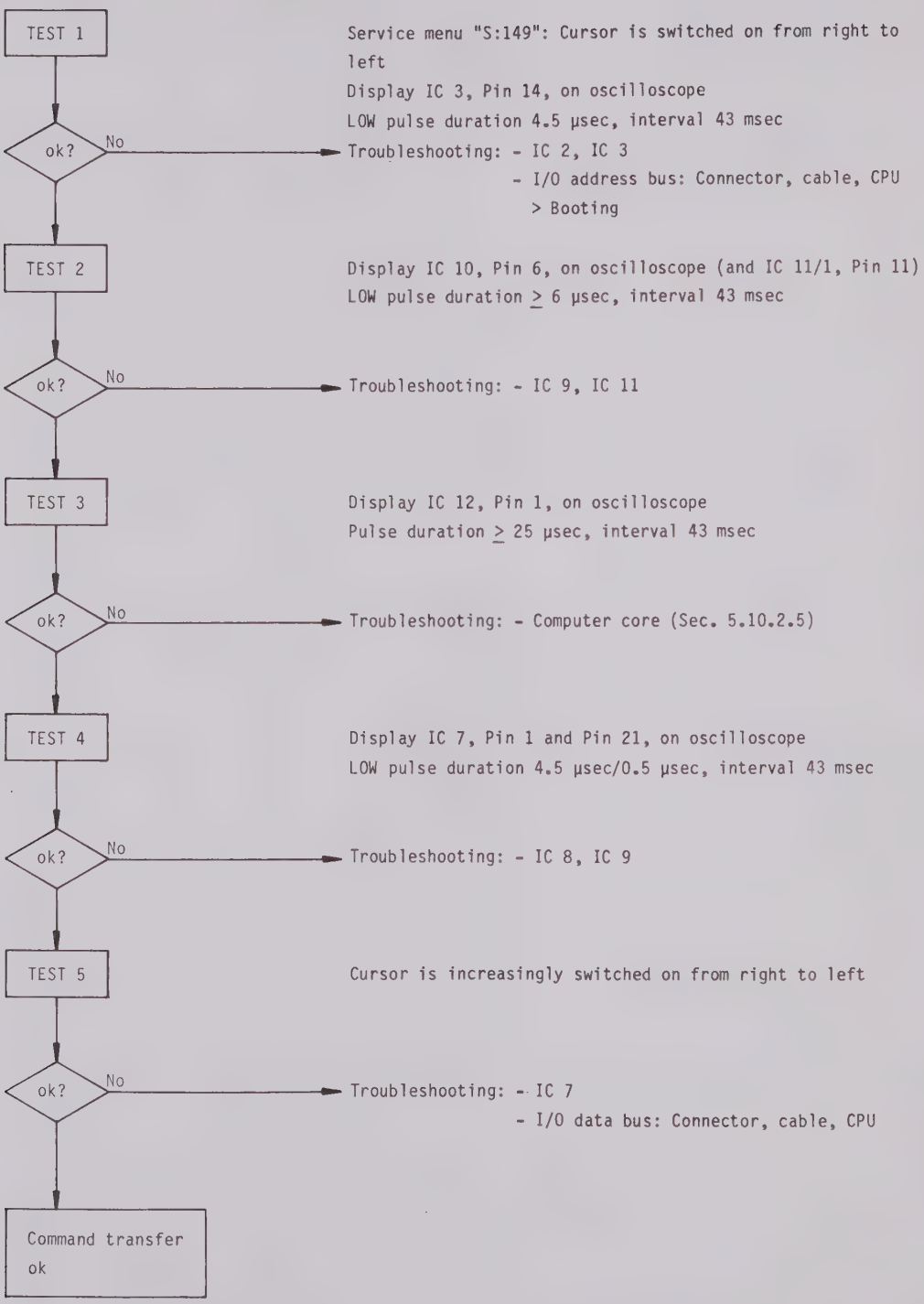
  GND -> EPROM 16, IC 15, Pin 14 (GND)
  Clock -> EPROM 16, IC 15, Pin 20 (ALE)
  Start -> EPROM 16, IC 15, Pin 27 (AR14)
  Stop -> EPROM 16, IC 15, Pin 27 (AR14)

- Signature recording

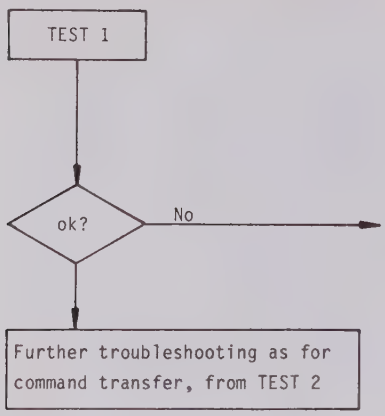
  Test probe on EPROM 16, IC 15, Pin 11 (DØ)
  Pin 12 (D1)
  Pin 13 (D2)
  Pin 15 (D3)
  Pin 16 (D4)
  Pin 17 (D5)
  Pin 18 (D6)
  Pin 19 (D7)

  Compare the display value with the glued-in signature list

5.10.2.6 Troubleshooting, command transfer



5.10.2.7 Troubleshooting, data transfer



Service menu "S:143"
Entire character generator contents (large, upper, lower) are displayed from left to right
Display IC 3, Pin 13, on oscilloscope (or logic test probe TKL 515)
LOW pulse duration 4.5 µsec, interval 170 msec
Troubleshooting: - IC 2, IC 3
- I/O address bus: Connector, cable, CPU
> Booting

5.11 POWER SUPPLY UNIT (N)

5.11.1 OPERATING VOLTAGES

The analog operating voltages can be checked in the carrier phase meter (6) [2019-Q].

The carrier phase meter and its test points are accessible after removing the lower housing section.

-5.2 V* at Pt. 4
+12 V at Pt. 5
-12 V at Pt. 6
+5 V at Pt. 2

* The -5.2 V are derived from the -6.2 V, meaning that the -6.2 V supply voltage is checked at the same time.

5.11.2 TROUBLESHOOTING IN THE POWER SUPPLY UNIT

If the power supply unit is disconnected from the instrument - the DC/DC converters idle - the output voltages can run up or the converters oscillate. Correct information on the outpt voltages can only be obtained with the converters loaded.

In this case, the following minimum load will suffice (see Fig. 5.11-1):

+12 V approx. 120 mA: resistor 100 Ω 4 W Bu eL or M
-12 V approx. 120 mA: resistor 100 Ω 4 W Bu eS or R
+5 V approx. 150 mA: resistor 33 Ω 4 W Bu eI or e8
-6.3 V approx. 190 mA: resistor 33 Ω 4 W Bu e7, H

The -5.2 V linear controller can be operated in idle state.

When measuring the assemblies, converters can be removed for troubleshooting if no load is used. The converters which can be removed are stated in each case.

When using the auxiliary load (see Fig. 5.11-1), combine all ground connections via connecting plugs: e6, 9, 11, 12, 13, 14, D, E, F, k, N, P. From Series B onwards, a battery board with three 1.2 V, 180 mA/h storage batteries must be connected via socket e2 -> ground.

The switching point for the data-save function is stated as > 180 V < 180 V~ . However, this only applies when the power supply unit is under load. The high-end voltage is the determining factor, i.e. with the above load, the mains voltage is 137 V or 146 V~ at the 17.5 V and 19 V switching points. The ripple voltage is approx. 0.25 V_{pp} and is negligible.

Auxiliary equipment:

1 Battery board [2019-AX]
1 Comb plug [2019-AS]* } Auxiliary load**
2 Cement resistors, 100 Ω 4 W* } Auxiliary load**
2 Cement resistors, 33 Ω 4 W* } Auxiliary load**
1 Oscillograph with test probe
3 AC/DC multimeters
1 Variable-ratio transformer

* Fit ground lines and cement resistors as per Fig. 5.11-1

** The auxiliary load can also be ordered as a complete unit from the factory
Order No. 44-2019/2019-6500.067

Auxiliary load**

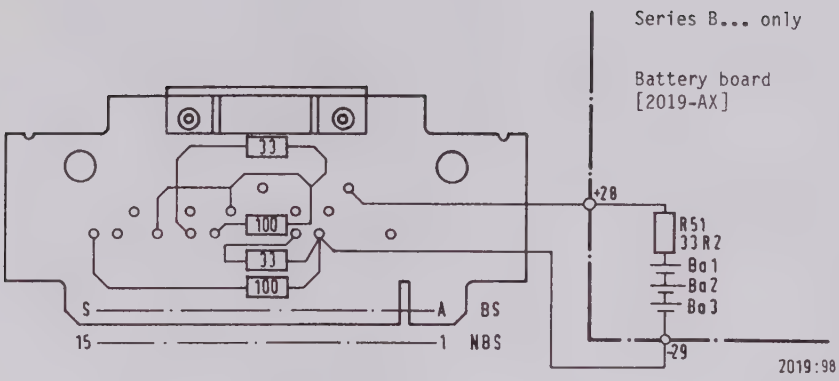


Fig. 5.11-1 Comb plug [2019-AS] as test device

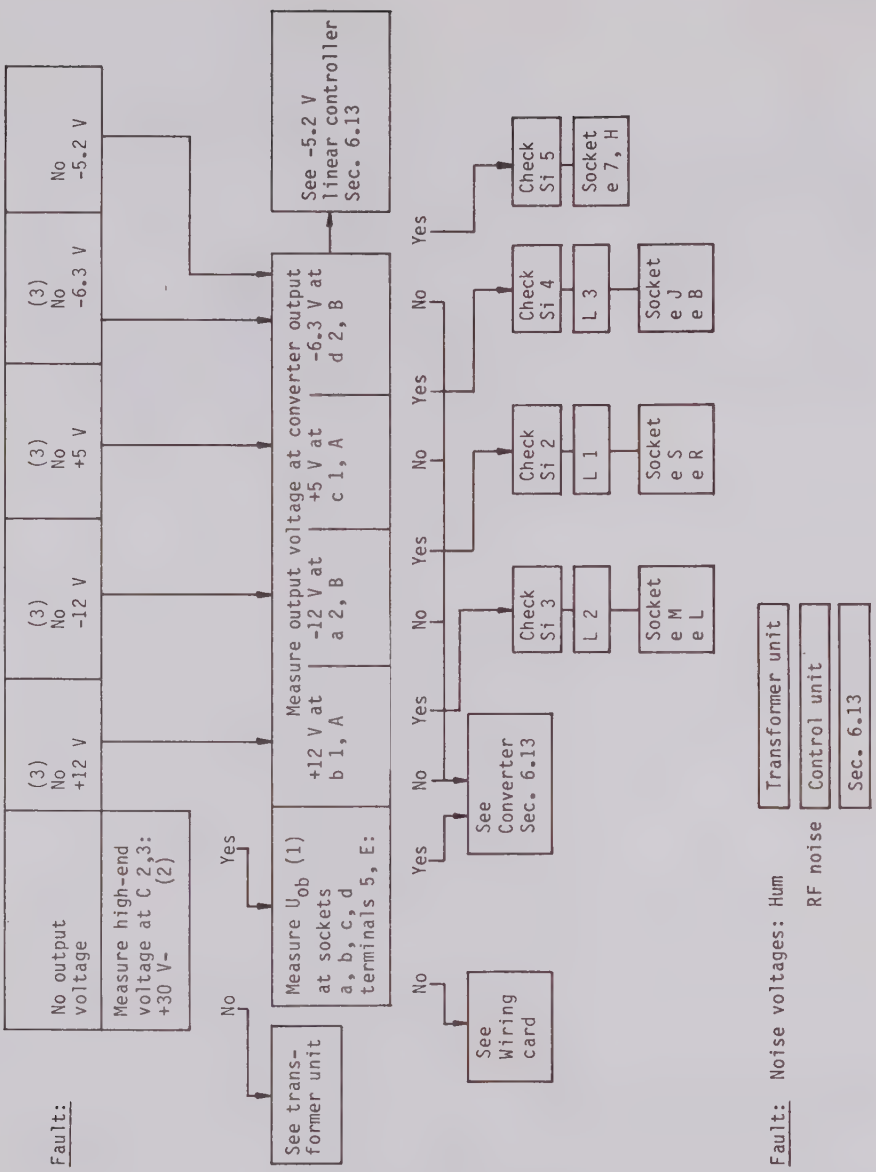


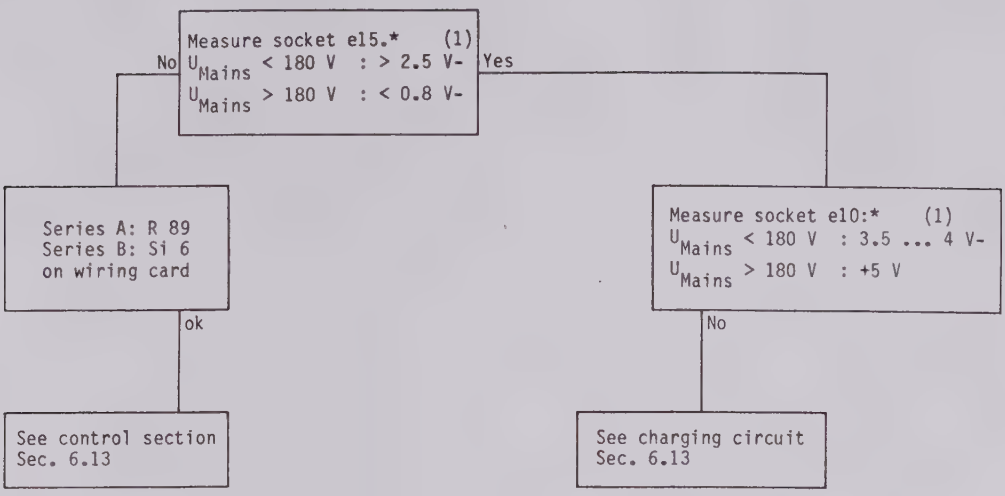
Fig. 5.11-2 Troubleshooting diagram, power supply unit

(1) Only socket c 5, E is accessible from the outside. However, if it is measured at this point, it can be assumed that U_{ob} is also present at the other sockets.

(2) The high-end voltage is approx. 30 V for the power supply unit without load.

(3) If the deviation is > $\pm$ 0.2 % -> Check the sync. voltage! (Section 6.14.5)

Fault: Data-save function does not work



* On wiring card [1/2019-AP]

(1) For power supply unit without load: approx. 140 V (135 and 145 V)

6 TROUBLESHOOTING: LOCALIZATION TO FAULTY COMPONENT 6-1

6.1 General notes on troubleshooting and repairs 6-1
6.2 Troubleshooting in the carrier oscillator [5/2019-P] 6-1
6.3 Troubleshooting in the carrier phase meter [6/2019-Q] 6-1
6.4 Troubleshooting in lock-in oscillator [6/2019-R] 6-2
6.5 Troubleshooting in the 220 MHz VCO [7/2019-M] 6-2
6.6 Functional check of controller 2 [7/2019-N] 6-3
6.7 Sawtooth phase meter [7/2019-O] 6-5
6.7.1 Functional check 6-5
6.7.2 Troubleshooting 6-11
6.7.3 Repairs 6-12
6.8 Mixer [7/2019-U] 6-12
6.8.1 Level check 6-12
6.8.2 Notes on troubleshooting 6-13
6.9 11 MHz phase meter [8/2019-G] 6-13
6.9.1 Notes on troubleshooting 6-13
6.9.2 Repairs 6-13
6.10 Troubleshooting in the 11 MHz VCO [8/2019-J] 6-13
6.11 Functional check, controller 1 [9/2019-H] 6-14
6.12 Troubleshooting the CPU-2, BN 965, circuit diagram (90) 6-16
6.12.1 Service switches 6-16
6.12.2 Troubleshooting with the aid of the self-test 6-17
6.12.2.1 Cyclic tests on the CPU-2 6-17
6.12.2.2 Description of test programs 6-18
6.12.3 Troubleshooting with the aid of signature analysis 6-20
6.12.3.1 Troubleshooting in the event of a ROM fault 6-22
6.12.3.2 Adress signatures 6-23
6.12.3.3 Troubleshooting in the event of a RAM fault 6-24
6.13 Troubleshooting the IEEE 488/<IEC 625> Interface bus card BN 958, circuit diagram (91) 6-25
6.13.1 Introduction 6-25
6.13.2 Extra device-specific test 6-25
6.14 Troubleshooting in the power supply unit 6-26
6.14.1 Transformer unit 6-26
6.14.2 Wiring card 6-26
6.14.3 -5.2 V linear controller 6-26
6.14.4 Charging circuit 6-27
6.14.5 Control unit 6-28
6.14.6 DC/DC modules 6-29

6 TROUBLESHOOTING: LOCALIZATION TO FAULTY COMPONENT

6.1 GENERAL NOTES ON TROUBLESHOOTING AND REPAIRS

Section 6 covers the following:

- The circuits of the functional groups: (A) Frequency generator
  (D) 220 MHz circuit
  (E) 11 MHz circuit
- It does not cover: Circuits forming a functional group of their own; e.g. adder, code error card. Refer to Section 5 for such circuits.

Further assistance in troubleshooting:

Circuit-related block circuit diagram, Section 10
Circuitry descriptions, Section 9

For repairing circuits, specifically the phase meter:

After repairing a circuit, it is usually necessary to carry out or check an alignment.

For this reason, the 11 MHz phase meter should only be repaired under certain circumstances. Depending on the nature of the repair, it may be necessary to check the linearity in order to guarantee measuring accuracy. These linearity checks can only be performed in the factory.

Consequently, it is advisable to replace a faulty 11 MHz phase meter. Please observe the corresponding note in Section 6.9.

6.2 TROUBLESHOOTING IN THE CARRIER OSCILLATOR [5/2019-P]

Check the level and frequency as per the alignment instructions in Section 7.2.1.1.2.
For further troubleshooting, refer to the circuitry description in Section 9.2.1.1.

6.3 TROUBLESHOOTING IN THE CARRIER PHASE METER [6/2019-Q]

Fault: Incorrect carrier frequency with internal bit rate setting (see Section 5.1.1, TEST 3)

Troubleshooting:
- Check the input signals: Section 5.1.1 TEST 1 Lock-in oscillator
  TEST 2 Carrier oscillator
- Check the "SYN. INT. EXT." control signal:
  Via the "ENTW" test menu, switch between INTERNAL and EXTERNAL in the "TRPH-MESSER" menu and observe the control signal at 6 Pt. 3.
- Check the circuit function: Section 9.2.1.2

Fault: Faulty external clock synchronization (see Section 5.1.1, TEST 3)

Troubleshooting:
- Check the clock divider output signal [6/2019-S]:
  f = ext. clock frequency/10
- Check the lock-in oscillator frequency: 22 MHz
- Check lock-in aid switching 6 T 4: Section 9.2.1.2
- Further circuit checks:
  Mixer 6 IC 5, 17 MHz LP filter, comparator 6 IC 1

Fault: Excessive phase noise (inherent jitter)

Troubleshooting:
- Check lock-in oscillator level: Section 5.1.1, TEST 1 Lock-in oscillator
- Check offset alignment 6 P 1: Section 7.2.1.2.1
- Possibly replace phase meter 6 IC 2

6.4 TROUBLESHOOTING IN LOCK-IN OSCILLATOR [6/2019-R]

Fault: No output signal (see Section 5.1.1, TEST 1)

Troubleshooting:
- Check driver/decoder function 6 IC 102
- Crystal circuit T 102/103
- Check resonant circuit alignment: Section 7.2.1.3

Fault: Excessive phase noise (inherent jitter)

1. At all bit rates:

   Troubleshooting:
   - Operating voltage interference, Section 4.5.3.2
   - Voltage filter 6 IC 1
   - Check resonant circuit alignment: Section 7.2.1.3.1

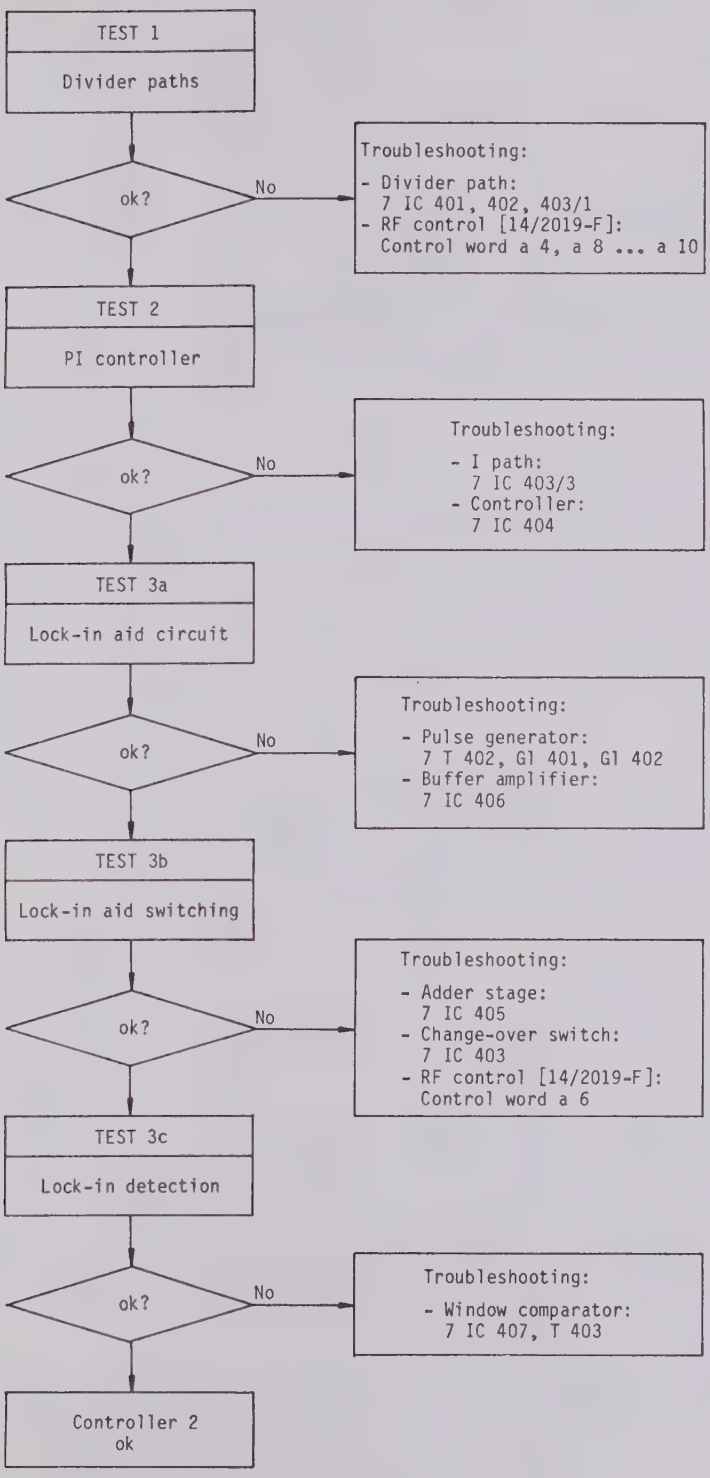
2. At one bit rate:

   Troubleshooting:
   - Check crystal mount (crystal loose?)
   - Check alignment -> tuning voltage Section 7.2.1.3.2
   - Swap crystal by way of experiment

6.5 TROUBLESHOOTING IN THE 220 MHz VCO [7/2019-M]

Check the level and frequency as per the alignment instructions in Section 7.2.4.1.
For further troubleshooting, refer to the circuitry description in Section 9.2.4.1.

6.6 FUNCTIONAL CHECK OF CONTROLLER 2 [7/2019-N]



TEST 1: Divider paths

Feed the PJM-4 with a 34.368 Mbit/s clock signal from the PJG-4.
In controller 2, open switch S 401 and connect 7 Pt. 46 to ground.
In the "RAST-EINST" menu of the "ENTW" test menu: - Set RASTHILFE "EIN"
- Select "REGELGRENZFREQUENZ" menu
Use the oscilloscope to test the sawtooth oscillation at input 7 Pt. 42:
u = approx. 700 mV_{pp}
If there is no oscillation: Troubleshooting as per Section 5.4.1.

Set the control limit frequencies consecutively and test the oscillation amplitude with the oscilloscope at the divider output (base of 7 T 401):

Setting/kHz	500	240	150	60	25	12	6	2
Amplitude/mV_{pp} approx..	700	340	210	80	35	16	8	$\leq$ 2

TEST 2: PI controller

Operate the PJM-4 without an input signal.
In the "RAST-EINST" menu of the "ENTW" test menu, set RASTHILFE "AUS".

1. Use a DVM to measure at 7 IC 404, Pin 2 and Pin 3:
   $U_2 = U_{\varphi 2}$ (7 Pt. 42) $\pm$ 5 mV
   $U_3 = U_{REF2}$ (7 Pt. 41) $\pm$ 5 mV
2. On 7 IC 404, connect Pin 2 and Pin 6:
   $U_{2,6} = U_{REF2}$ (7 Pt. 41) $\pm$ 5 mV

TEST 3: Lock-in aid

Operate the PJM-4 without an input signal.
In controller 2, open switch S 401 and connect 7 Pt. 46 to ground.
In the "RAST-EINST" menu of the "ENTW" test menu, set RASTHILFE "EIN".

Use the oscilloscope to test the sawtooth oscillation at input 7 Pt. 45:
u = approx. 2.5 V_{pp}
f $\leq$ 1 kHz
If there is no oscillation: Troubleshooting as per Section 5.5.1
If f > 1 kHz: Re-align 220 MHz VCO as per Section 7.2.4.1.1

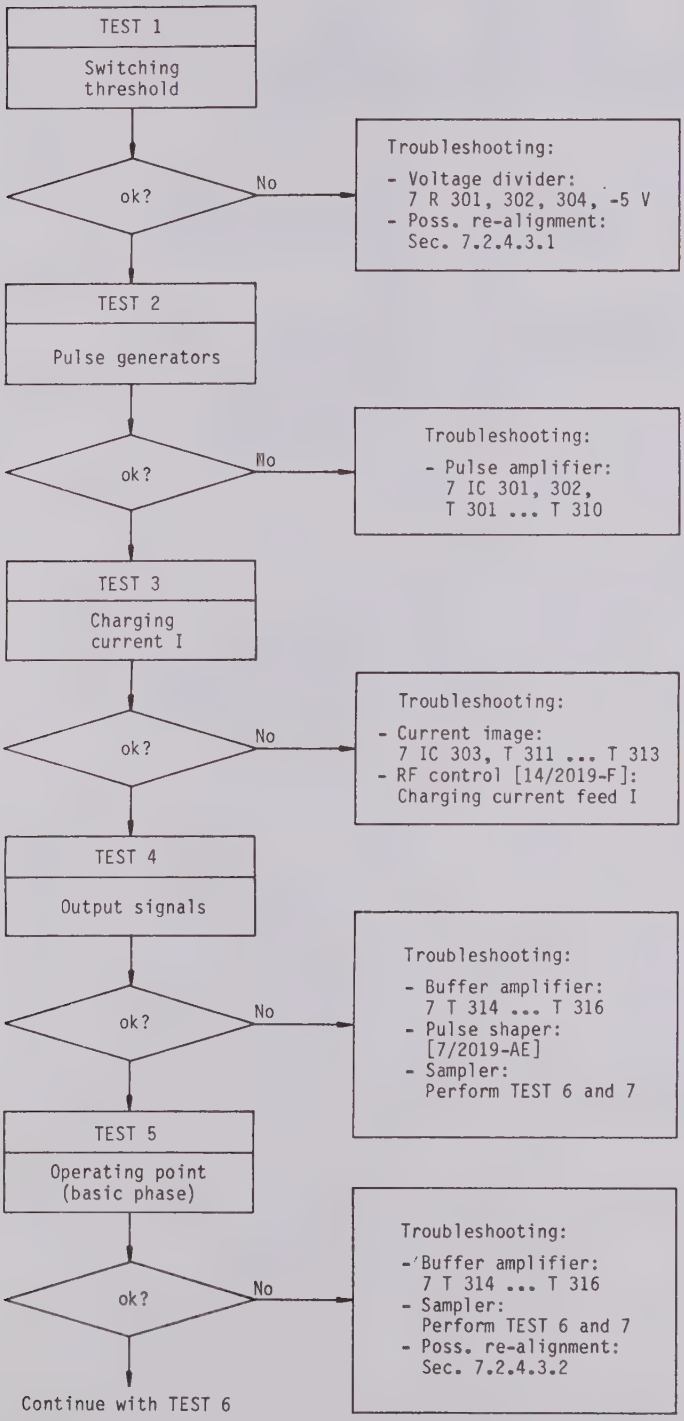
TEST 3a: Test the signal at 7 IC 406, Pin 6:
DC level : U = U_{REF1} (7 Pt. 44)
AC signal: pos. or neg. pulses, approx. 1.5 V_p

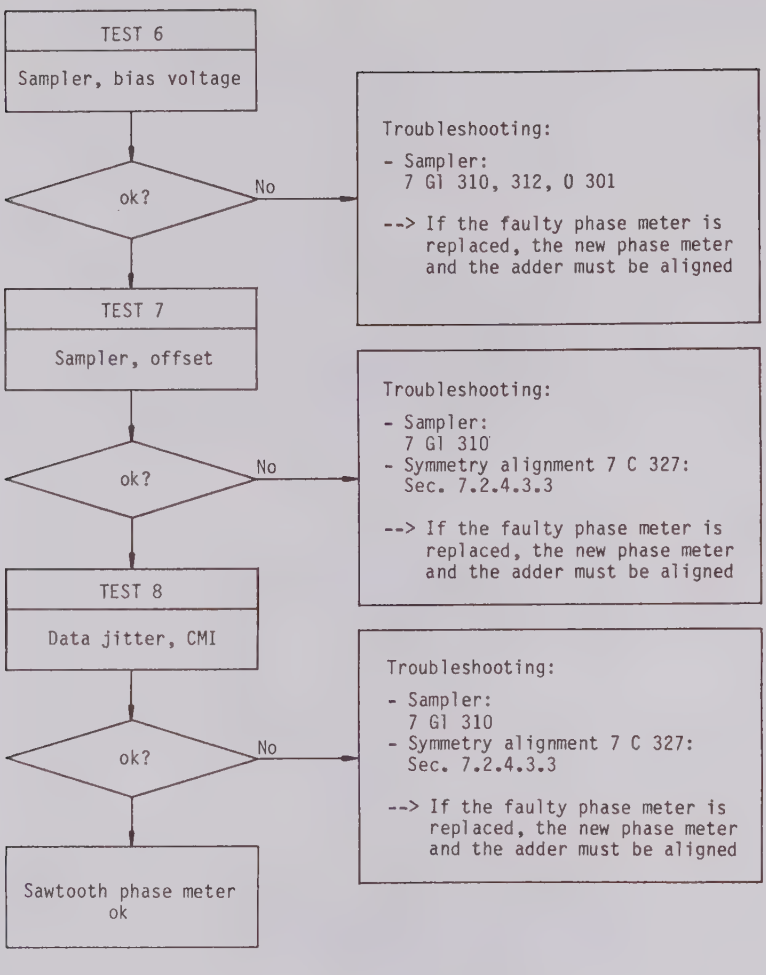
TEST 3b: Test the signal at output 7 IC 403, Pin 4:
DC level : U = U_{REF2} (7 Pt. 41) $\pm$ 100 mV
AC signal: Sawtooth oscillation, approx. 1.7 V_{pp}

TEST 3c: Test the pulses at output 7 a 5:
TTL LOW pulses, T_{LOW} approx. 5 µs

6.7 SAWTOOTH PHASE METER [7/2019-0]

6.7.1 FUNCTIONAL CHECK




TEST 6
Sampler, bias voltage
ok?
No
Troubleshooting:
- Sampler:
7 G1 310, 312, 0 301
--> If the faulty phase meter is replaced, the new phase meter and the adder must be aligned
TEST 7
Sampler, offset
ok?
No
Troubleshooting:
- Sampler:
7 G1 310
- Symmetry alignment 7 C 327:
Sec. 7.2.4.3.3
--> If the faulty phase meter is replaced, the new phase meter and the adder must be aligned
TEST 8
Data jitter, CMI
ok?
No
Troubleshooting:
- Sampler:
7 G1 310
- Symmetry alignment 7 C 327:
Sec. 7.2.4.3.3
--> If the faulty phase meter is replaced, the new phase meter and the adder must be aligned
Sawtooth phase meter ok

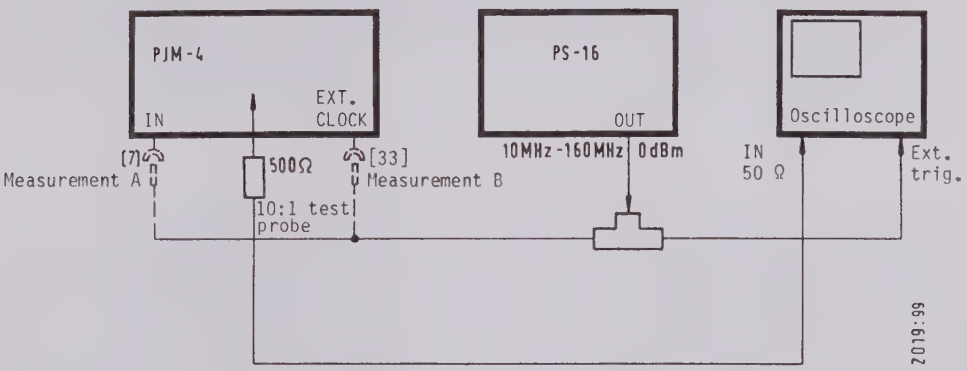
TEST 1: Switching threshold

Test as per the alignment instructions in Section 7.2.4.3.1

TEST 2: Pulse generators

Measuring instruments: 1 Generator 10 - 160 MHz e.g. PS-16 W&G
1 Oscilloscope BW > 300 MHz e.g. 2465 Tektronix
(Ideal: Sampling oscilloscope, BW > 1 GHz)
1 Power divider 75 Ω

Test setup:



A) Test of the sampling pulse generator:

Feed PJM-4 input [7] with the generator signal
PJM-4 settings: CLOCK, 139 Mbit/s
Other settings as desired

Vary the generator from 10 MHz to 160 MHz.
Use a 500 Ω test probe and ground spring to measure the pulse signal across 7 R 315 (= collector of T 305).

B) Test of the sawtooth pulse generator:

Apply the generator signal to EXT. CLOCK input [33]
PJM-4 settings: Bit rate EXTERNAL
Other settings as desired

Vary the generator from 10 MHz to 160 MHz.
Use a 500 Ω test probe and ground spring to measure the pulse signal across 7 R 332 (= collector of T 310).

Required values: See oscillograms

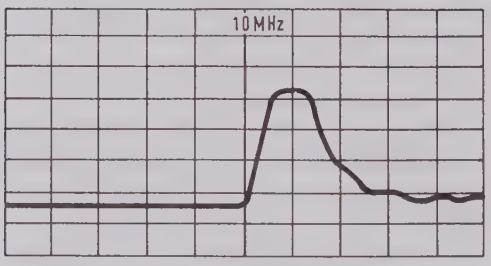
Max. permissible amplitude deviation : $\pm$ 20 %
Max. rise time : $\leq$ 1 ns
(Note inherent rise time of oscilloscope)

Oscillograms, sawtooth phase meter

Sampling pulse gen.

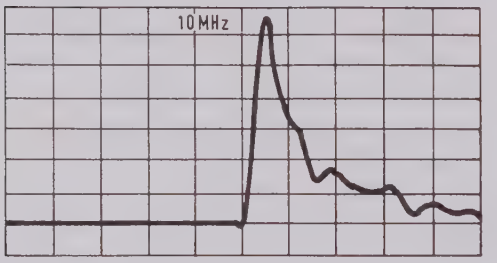
Measured with HP 54100 + 500 Ω 10:1 test probe
2 V/Div, 2 ns/Div

Coll. T 303

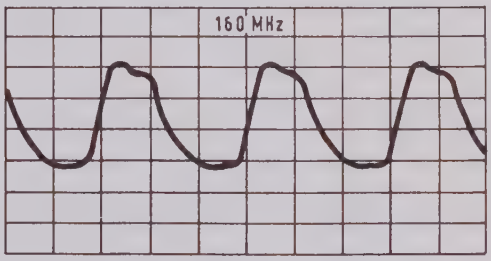


Coll. T 304

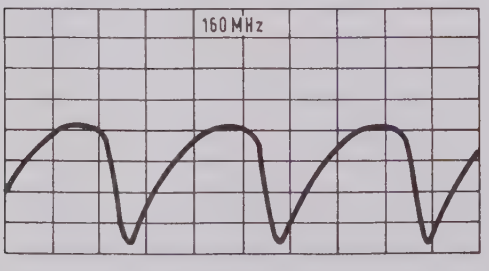
Coll. T 305



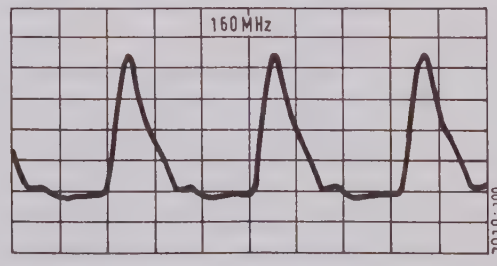
Coll. T 303



Coll. T 304



Coll. T 305

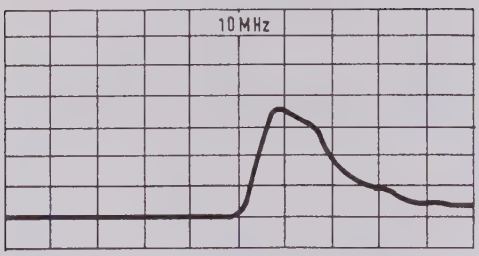


2019.100

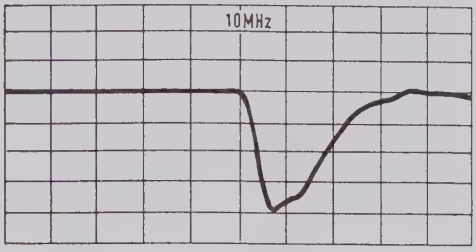
Sawtooth pulse generator

Measured with HP 54100 + 500 Ω 10:1 test probe
2 V/Div 2 ns/Div

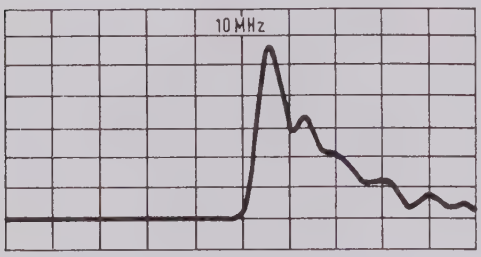
Coll. T 308



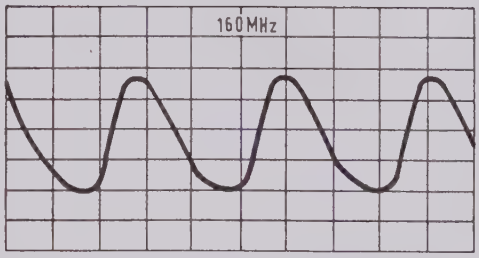
Coll. T 309



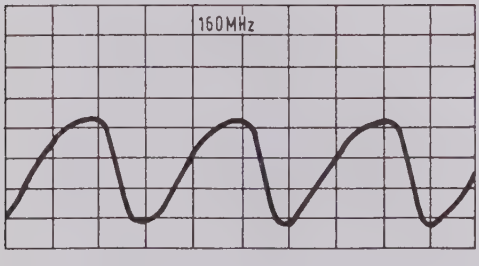
Coll. T 310



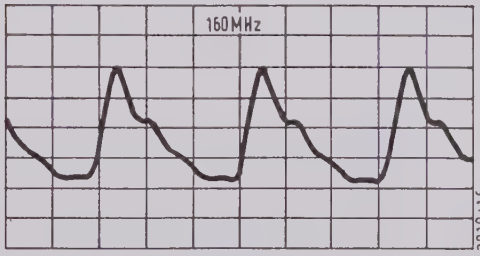
Coll. T 308



Coll. T 309



Coll. T 310



2019:16

TEST 3: Charging current $I_{\varphi s}$

On the PJM-4, call up the "PRUEFFELD" menu (see Sec. 9.3) and set 4.6 mA in the STROMQUELLE menu.

Use the DVM to measure the voltage across 7 R 372:

U = 460 mV $\pm$ 10 mV

Use the DVM to measure the voltage across 7 R 340 and 7 R 341:

U = 4.6 V $\pm$ 0.1 V

After the test, select AUTO in the TRAEGERPHASENMESSER menu to return to normal operation.

TEST 4: Output signals

Feed the PJM-4 with a clock signal from the PJG-4.

For measuring in the unlocked state, open the Dip-Fix switch 7 S 401 in (7) Controller 2 and connect control voltage output Pt. 46 to ground with a crocodile clip.
The measurement in locked-in state serves as a check only, since locking-in is usually impossible in the presence of a fault.

Measure the following in (7) Controller 2 (due to better accessibility):
1. With oscilloscope: AC signal (sawtooth oscillation) at:

	7 Pt. 43 ($U_{\varphi 2}$)	Frequency
Locked	Crosstalk of sawtooth oscillation: < 100 mV_{pp}	Bit rate
Unlocked	Sampled sawtooth oscillation: 400 - 500 mV_{pp} Bit rate = 139 Mbit 630 - 770 mV_{pp} Bit rate < 35 Mbit	f < 100 kHz

2. With digital voltmeter: DC values at:

	7 Pt. 41 (U_{REF2})	7 Pt. 43 ($U_{\varphi 2}$)
Locked	1 ... 3 V	U_{REF2} $\pm$ 2 mV
Unlocked	1 ... 3 V	U_{REF2} $\pm$ 40 mV

3. Sawtooth oscillation at 2 Mbit/s setting (unlocked):

The oscillation must not be limited.

TEST 5: Operating point (basic phase)

Feed the PJM-4 with a clock signal from the PJG-4.

Check the operating point as per the alignment instructions in Section 7.2.4.3.3 for all bit rates common to the PJG-4 and PJM-4:

139 Mbit/s: Symmetrical limitation at approx. 0.7 UI

< 35 Mibt/s: No limitation or unlocking up to approx. 0.8 UI

TEST 6: Sampler bias voltage

Feed the PJM-4 with a clock signal from the PJG-4.

Connect the sampler input to ground directly at Pt. 1 of the pulse shaper [2019-AE].
Use the DVM to measure the DC voltage at 7 0 301 Pt. 2 and Pt. 3:

Required: U_3, U_4 > 1 V (at all bit rates)
$|U_3 - U_4|$ < 400 mV

TEST 7: Sampler offset

Operate the PJM-4 with a clock signal (1 MHz ... 160 MHz, 0 dBm) from a sine-wave generator, e.g. PS-16.

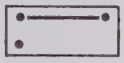
PJM-4 setting: Bit rate EXTERNAL (do not supply an external clock!)
Other settings as desired

Connect the DVM to output 7 TP 4 (U_{REF2}) and 7 TP 5 ($U_{\varphi 2}$).
Slowly adjust the generator from 1 MHz to 160 MHz and determine the minimum and maximum differential voltage occurring between TP 4 and TP 5:

Required: $U_{max} - U_{min}$ < 80 mV

TEST 8: Data jitter, CMI

Feed the PJM-4 with a data signal from the PJG-4.

In the sawtooth phase meter, connect the pulse shaper input [2019-AE], Pt. 5, to ground with a short connection.
In adder [10/2019-AF], flip the Dip-Fix switch 10 S 3 (11 MHz path OFF). 

Settings:

PJG-4: - CMI, 139 Mbit/s, random sequence 2^{23}-1 or other bit rate/code combination to be tested
- Modulation OFF

PJM-4: - Call up testprogram BASIC NOISE (see section 4.5.3.1)
- Bit rate 34.368 Mbit/s; this setting applies regardless of the bit rate set
- HP = 2 Hz, LP = 6700 kHz
- Code: To match the PJG-4 signal
- Via the "ENTW" test menu, set the following:
in the "TRPH-MESSER" menu : "EXTERN" carrier phase meter
in the "STROMQUELLE" menu : 0 mA
in the "RAST-EINST" menu : Lock-in aid "EIN"
- Press the "RETURN" key to return to the measuring program (display)

Note: If the bit rate on the PJM-4 is switched over, the "EXTERN" carrier phase meter setting must be repeated.

Required display: < 20 mUI_{pp}

6.7.2 TROUBLESHOOTING

Fault: Lock-in problems in the 220 MHz circuit or no sawtooth phase meter output signal
Troubleshooting: Perform the functional check as per Section 6.7.1

Fault: 90° basic phase alignment or delay alignment for code error circuit faulty
Troubleshooting: Section 6.7.1 TEST 4 Output signals
TEST 5 Operating point
TEST 7 Sampler offset
TEST 2 Pulse generators

Fault: Excessive inherent jitter at 139 Mbit/s, CMI:
Troubleshooting: Section 6.7.1 TEST 8 Data jitter, CMI
TEST 1 Switching threshold
TEST 2 Pulse generators

Fault: Excessive inherent jitter, regardless of bit rate and code:
Troubleshooting:
- Check charging current $I_{\varphi s}$ for noise:
  Current image 7 IC 303, T 311 ... T 313
  Current source on RF control [14/2019-F]
- Check level of regenerated clock:
  Section 5.4.1 TEST 1 Regenerated clock
- Check switching threshold:
  Section 6.7.1 TEST 1 Switching threshold

6.7.3 REPAIRS

Repairs should only be carried out in the area of the pulse generators and the buffer amplifier.

Repairs in the area of the sampler Gl 310, D 301, Gl 312 and the pulse shaper [2019-AE] necessitate symmetry alignment as per Section 7.2.4.3.2.

The following should be checked after all repairs:
- Alignments as per Sections 7.2.4.3.1 and 7.2.3.3; if faulty: re-align
- Alignment as per Section 7.2.4.3.2; if faulty, re-align

6.8 MIXER [7/2019-U]

6.8.1 LEVEL CHECK

Operate the PJM-4 without an input signal.

In (7) Controller 2, open Dip-Fix switch 7 S 401 and connect control voltage output Pt. 46 to ground using a crocodile clip.

Select the bit rates available in the instrument consecutively. Use an analyzer and active test probe (e.g. TEK 495A and TEK P6201) to check the levels in mixer [7/2019-U]:

Test point	Set bit rate	Measured values	
		Level	Frequency
7 Pt. 12	Any	Approx. -6 dBm	220 MHz
7 Pt. 11	2.048 Mbit/s 139.264 Mbit/s	Approx. -5 dBm Approx. -2 dBm	222.048 MHz 359.264 MHz
Mixer output 7 Pt. 8	8.448 Mbit/s 139.264 Mbit/s	Approx. -18 dBm Approx. -22 dBm	8.448 MHz 139.264 MHz
Mixer output 7 Pt. 9	8.448 Mbit/s 139.264 Mbit/s	Approx. -14 dBm* Approx. -10 dBm*	8.448 MHz 139.264 MHz

* The levels depend on the alignment of 7 C 106

6.8.2 NOTES ON TROUBLESHOOTING

Fault: 90° basic phase adjustment faulty (see Section 5.3.1, TEST 4)

Troubleshooting:
- Maximize the level at 7 Pt. 9 with 7 C 106:
  Perform a level check as per Section 6.7.1
- Re-align as per Section 7.2.4.4.1:
  If the level at 7 Pt. 9 drops by more than 6 dB, also check the following circuits: -> Code error [3/2019-AL]
  -> Sawtooth phase meter [7/2019-0]

6.9 11 MHz PHASE METER [8/2019-G]

6.9.1 NOTES ON TROUBLESHOOTING

Fault: Output signals faulty (see Section 5.5.1, TEST 4)

Troubleshooting: With the aid of the circuitry description in Section 9.2.5.1

Fault: Excessive inherent noise (see Section 5.5.4)

Troubleshooting: Swap phase meter. Remember to re-align the adder!

Fault: Faulty frequency response (see Section 5.5.2.2)

Troubleshooting: Swap phase meter. Remember to re-align the adder!

6.9.2 REPAIRS

It is not advisable to repair the limiter amplifier, since the possible necessary alignment of 8 P 2 necessitates a linearity check, which can only be performed in the factory.

6.10 TROUBLESHOOTING IN THE 11 MHz VCO [8/2019-J]

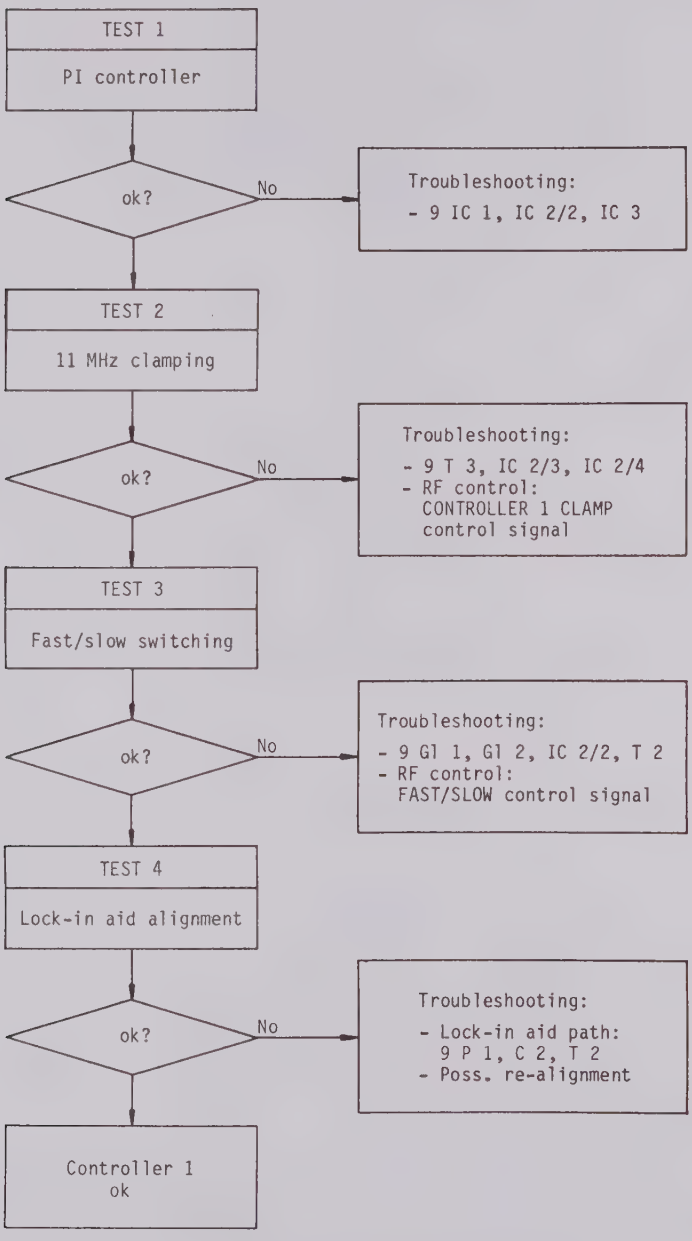
Fault: Faulty VCO output signal (see Section 5.5.1, TEST 3)

Troubleshooting: With the aid of the circuitry description in Section 9.2.5.3

Fault: Excessive inherent jitter (see Section 5.5.4, Testing the uncontrolled VCO with the test setup as per Section 4.7.1.2, Measurement 2)

Troubleshooting: The following should be checked:
- The crystal must be secured firmly by the retaining clips on both sides (!).
- All components, shims and spacers in the region of the crystal circuit must be checked for a tight fit.
- As an experiment, swap the crystal for one known to be good.
- Check the function as per the circuitry description.
- Swap the 11 MHz VCO.

6.11 FUNCTIONAL CHECK, CONTROLLER 1 [9/2019-H]



TEST 1: PI controller

Test as per Section 5.5.1:

TEST 6 Lock-in aid, 11 MHz circuit, control voltage U

TEST 7 Lock-in aid, 11 MHz circuit, tuning voltage

TEST 2: 11 MHz clamping

Operate the PJM-4 without an input signal.

In the "RAST-EINST" menu of the "ENTW" test menu (see Section 9.3), set the following:

- REGLER 1 "KLEMM"
- RASTHILFE "EIN"

Use the DVM to measure the tuning voltage at 9 Pt. 4:

Required: $-2\ V < U < +2\ V$

TEST 3: Fast/slow switching

Measuring instruments: TR 940 (W&G) or digital storage oscilloscope

Operate the PJM-4 without an input signal.

In the "RAST-EINST" menu of the "ENTW" test menu (see Section 9.3), set the following:

- REGLER 1 "FLINK"
- RASTHILFE "AUS"

Check the sawtooth oscillation at 9 Pt. 2 ($U_{\varphi 1}$): approx. 2.5 V_{pp};
if there is no oscillation: troubleshooting as per Section 5.5.1.

Connect the TR 940 or storage oscilloscope in Controller 1:

Channel A (DC, 2 V/Div) : 9 IC 2/1, Pin 14

Channel B (AC, 0.5 V/Div): via 10:1 test probe to drain connection 9 T 2

Use the "RAST-EINST" menu to check FLINK/TRAEGE switching as per Fig. 6.11-1 (also refer to the circuitry description, Section 9.2.5.2):

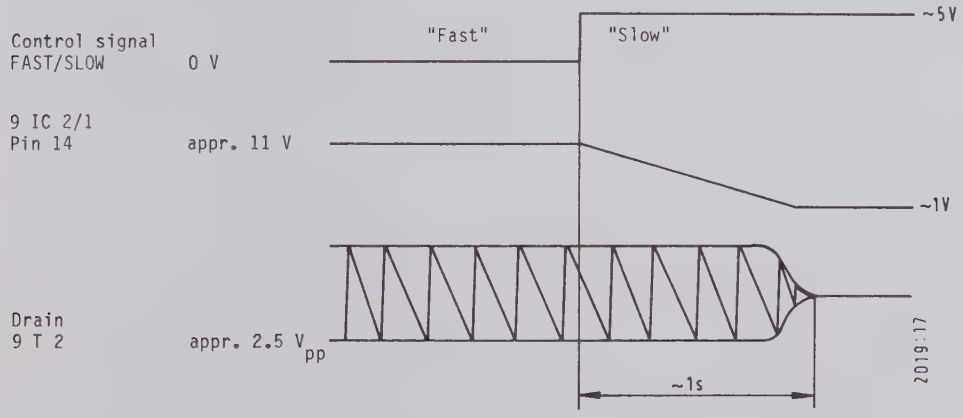


Fig. 6.11-1 Fast/slow switching operation

TEST 4: Lock-in aid alignment

Test as per the alignment instructions in Section 7.2.5.4.3.

6.12 TROUBLESHOOTING THE CPU-2, BN 965, CIRCUIT DIAGRAM (90)

6.12.1 SERVICE SWITCHES

The CPU-2, BN 965, contains a 10-pole DIL switch. Switches S 1/7 to 1/10 are required for the free-run function of the microprocessor, while switches S 1/1 to 1/6 are the actual service switches.

S1/	1	2	3	4	5	6	7	8	9	10
ON	o	o	o	o	o	o	•	•		•
OFF									•	

normal mode

service switch free-running switch

S1/	1	2	3	4	5	6	7	8	9	10
ON	any								•	
OFF							•	•		•

free-running mode

Note: The basic setting of switches S 1/1 to 1/6 may differ from that shown above, depending on the software used.

Fig. 6.12-1 Settings of the service and free-run switch S 1

The free-run switch is only required for signature analysis on the CPU.

NOTE: The arithmetic processor must be disconnected for free-running mode!

Service programs, such as continuous tests, single tests and stimulus programs, can be called up with the aid of the service switch. The code set causes the processor to establish the program start address in a table during initialization (after mains power-up via the data save input or the CLEAR input). The selected test or stimulus program is then executed once or cyclically. The service switch can be used to represent a 6-bit word, this allowing 64 different combinations.

6.12.2 TROUBLESHOOTING WITH THE AID OF THE SELF-TEST

(called up via DIL switch S 1)

6.12.2.1 Cyclic tests on the CPU-2

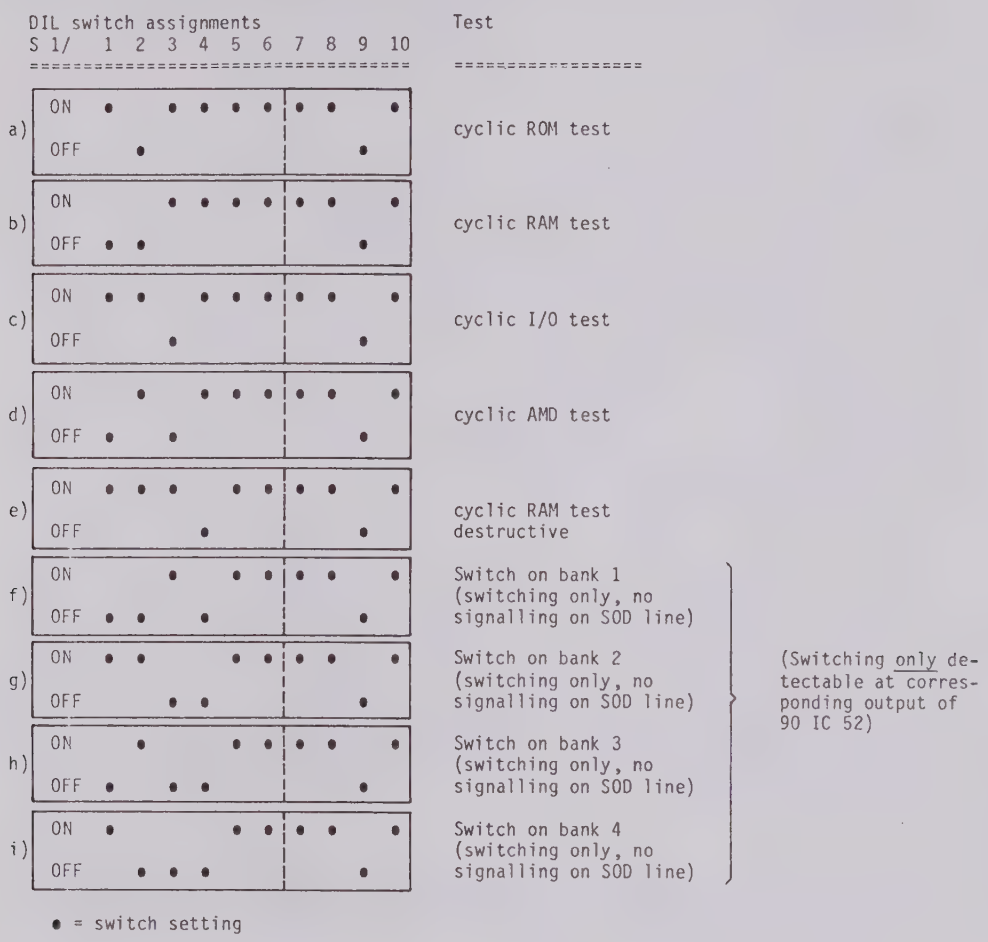


Fig. 6.12-2 DIL switch assignments

Test result: With oscilloscope at TP 2 (SOD): Frequency = Ø -< Faulty
Frequency ≠ Ø -< OK

6.12.2.2 Description of test programs

a) Cyclic ROM test

In the EPROM test, a 16-bit linear sum is formed across the memory contents and compared with the associated checksums previously determined by the checksum program and stored in the description list, starting at address 8ØH. If the checksums are not identical, a fault has occurred.

Memory content	Addition sequence		
D end	2	End address	(End)
D end-1	4	End address - 1	(End-1)
D sta+2	5	Start address + 2	(Start+2)
D sta+1	3	Start address + 1	(Start+1)
D sta	1	Start address	(Start)

Fig. 6.12-3 ROM test procedure - Addition of memory contents

S = (D sta) + (D end) + (D sta+1) + (D end-1) + (D sta+2) .....

EPROM test algorithm

The memory contents are added upwards from the start address of the EPROM and downwards from the end address of the EPROM.
This type of address change tests the address decoder adequately, since the address bit changes approximately simulate the real program sequence.

b) Cyclic RAM test

A non-destructive test of the RAM contents is performed on the instrument. The operating data, such as level and frequency settings, is retained.

This RAM test consists of two parts:

- Cell test for examining the individual memory cells
- Address test for examining the addressing of these memory cells

In the cell test, various bit patterns are written and read in order to establish whether interlinks exist between the individual bits and/or cells. All bit interlinks are detected, even without a knowledge of the internal RAM topology.

NOTE: A far more stringent test of address decoding can be performed using the "destructive" RAM test programs (see Item f)).

c) Cyclic test of the slow I/O bus

The I/O bus test checks the data lines of the slow I/O bus and detects short-circuits on the data lines (and on the device bus!).

The test function of the I/O bus is activated at the start of this program. This prevents further components connected to the I/O bus from writing data onto the I/O bus. The test consists of writing various data words onto the bus, reading them back in (IC 43) and comparing the written and read words. The write driver (IC 42) remains active during reading.

Path: Writing out -> IC 42 (I/O data latch)
Reading in via IC 44 (45) and IC 43

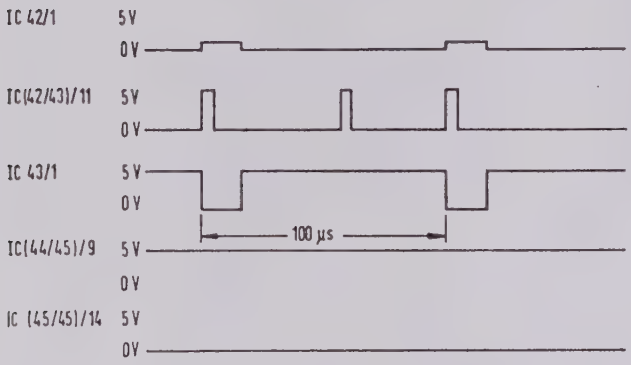


Fig. 6.12-4 I/O module activation

d) Cyclic test of the arithmetic module Am 9511

The test of the arithmetic module Am 9511 is called up if the arithmetic module is fitted on the CPU card. The test performs a simple calculation. The test is based on the assumption that either all calculations will be performed correctly, or none at all.
In this test program, all interrupts are disabled during program execution, since an even number of bytes must always be read out of the module in order not to produce an unacceptable change in the internal pointer of the module.

e) Cyclic RAM test "destructive"

This RAM test uses three algorithms and is thus a far more stringent address test than the non-destructive RAM test. The test includes the following:

- Forward address interlinks
- Backward address interlinks
- Decoder
- Stuck address lines
- Chip select logic
- State-changing behaviour of the bit cells

The scope of the individual test algorithms varies in relation to the different fault mechanisms. They also overlap in part.
For example, the switching of each bit cell to "zero" and "one" is tested by three algorithms, but with different degrees of severity.
The complete performance of the non-destructive RAM test and the three test algorithms of the "destructive" RAM test provide all the testing necessary.
The "destructive" RAM test can be used for troubleshooting and repair purposes, since the operating data do not have to be retained.

f) Free-running

Switch S 1 can be used to disconnect data lines AD$\emptyset$, AD6 and AD7 of the processor from the data bus. Thus, not all data bits output from the EPROM are passed to the processor.
During each read operation, the command code of a command triggering no activity is passed to the processor.
A more detailed explanation can be found in the next section "troubleshooting with the aid of signature analysis".

6.12.3 TROUBLESHOOTING WITH THE AID OF SIGNATURE ANALYSIS

The principle of signature analysis is described in Section 2.3 of this Service Manual. The CPU board has a free-running switch (S 1/7 to S 1/10) for this purpose. If the settings of S 1/7 to S 1/10 are inverted, the processor addresses the entire memory area by incrementing the address by 1 each time and performing this operation cyclically after a RESET. In order to record ROM signatures, the associated ROM select (test point) must be used as the START/STOP signal. The use of the free-running switch, in conjunction with the pull-up resistors of the data bus and the $\overline{RD2}$ signal via G1 2 to AD6, ensures that only a subset of the 8085 command set is executed.

Bit number :	7	6	5	4	3	2	1	$\emptyset$	
Logic level :	H	L	X	X	X	X	X	H	
Machine code:	1	$\emptyset$	X	X	X	X	X	1	= 81H..BFH

X = any, data line not disconnected.

Note: The free-running switch only affects data lines $\emptyset$, 6 and 7.

Fig. 6.12-5 Value of the data bits for free-running

The commands involved are one-byte commands for arithmetic or logic operations which increment the program counter reading by one and thus yield a "program" with consecutive memory addressing.

If the most-significant bit A15 is used as the START/STOP frame, and if the processor increments the entire address range (from $\emptyset\emptyset\emptyset\emptyset$H to FFFFH), each address line yields an unambiguous signature.

The free-running operation tests the heart of the microcomputer, namely

- a number of functions of the microprocessor and the circuits required for its operation, such as the clock generator circuitry,
- the address bus with drivers and decoders,
- the EPROM contents (including data bus), if the START/STOP frame is selected accordingly.

The I/O area and the RAMs cannot be tested in free-running mode.
The WORIS functions of the monitor program offer further testing capabilities.

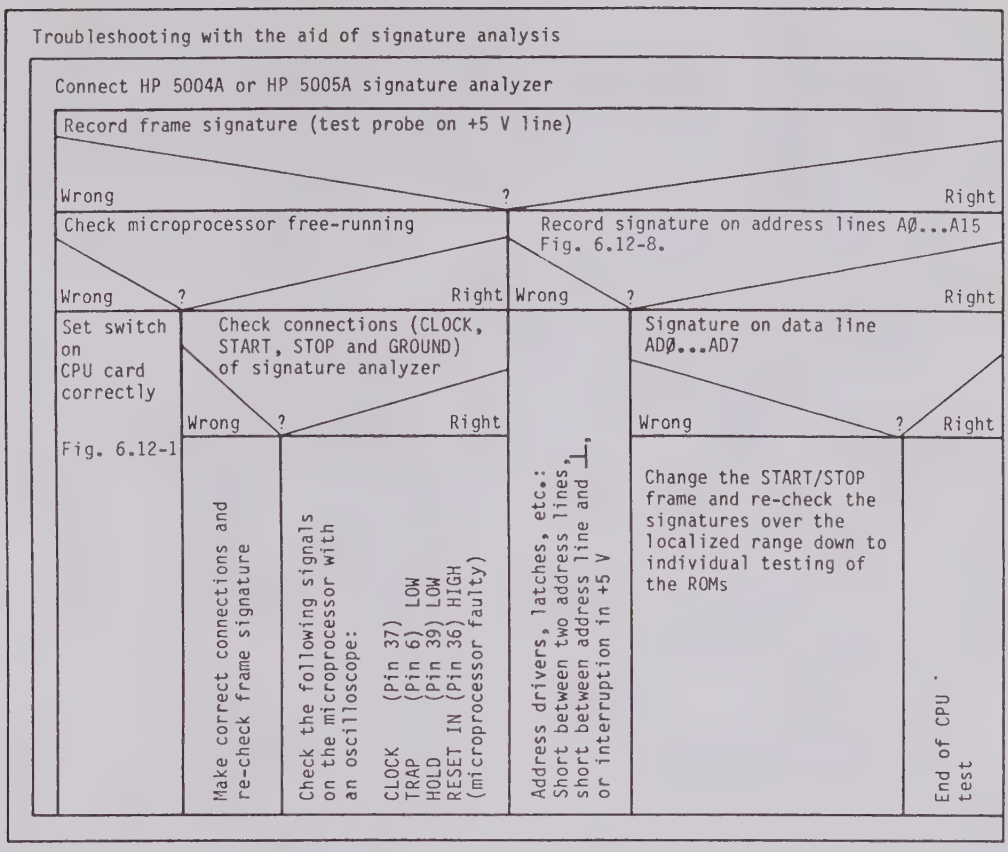


Fig. 6.12-6 Structural diagram of troubleshooting

6.12.3.1 Troubleshooting in the event of a ROM fault

Troubleshooting is performed with the aid of the Hewlett-packard signature analyzer 5004A or 5006A.*) Switches S 1/1 to S 1/10 on the CPU board must be set appropriately to activate the free-running mode (refer to CPU circuitry description for details). With the instrument switched off, set switch S 1 as shown in Fig. 6.12-1.

Measuring the data signatures:

Connect the signature analyzer:
Clock (⎍) at $\overline{RD}$: TP OE, GND to - pole C5

The signatures are checked at the outputs of the ROMs on the CPU board.

EPROM TP	IC	B.V.	START Connection	START Edge	STOP Connection	STOP Edge
ROMØØ	PL3	--	TP ROM ØØ	⎍	TP ROM ØØ	⎍

Fig. 6.12-7 Edge assignment of the START/STOP frame

As no memory switching occurs in free-run mode, ROMs Ø1 to Ø4 must be plugged into ROM socket ØØ for testing.

Checking the frame:

The signature 0000 must be obtained at Pin 20 (CE) of the EPROM in question, since this signal is always LOW during the selected frame. The characteristic signature must appear at Pin 20 of all other EPROMs, since these are not addressed and Pin 20 is thus constantly HIGH. The frame signature corresponds to the signature on the +5 V line.
Since minor software modifications, even if they only affect 1 bit, result in a different signature on the data lines, make sure that the correct signature list is consulted.
The signature list is attached to the instrument. The exact location of the list is described in Section 3 under the heading "Instrument data".
If none of the 8 signatures is correct, there is most probably a fault on the address side, in which case the signatures of the address lines must be checked.

*) Instruments from other manufacturers will not always produce the same signatures.

6.12.3.2 Address signatures

The address line signatures must be identical at all points. The signature on the CPU board, upstream and downstream of the address drivers and the address latches must be identical. If the signatures on ADØ...AD7 are to be checked, the trailing edge of the ALE signal must be used as the CLOCK. However, ADØ, AD6 and AD7 are only valid directly on the microprocessor in free-running mode. In addition to the signatures of the address lines, the signatures of the chip select signals = decoded addresses and of the enable signals must also be checked. The Table shown in Fig. 6.12-8 must be used for this purpose.

Test point	Signature
AØ (ADØ)*	UUUU
A1 (AD1)	5555
A2 (AD2)	CCCC
A3 (AD3)	7F7F
A4 (AD4)	5H21
A5 (AD5)	OAFA
A6 (AD6)*	UPFH
A7 (AD7)*	52F8
A8	HC89
A9	2H70
A1Ø	HPPO
A11	1293
A12	HAP7
A13	3C96
A14	3827
A15	755U
$V_Ø$	5FU8
V_1	29A6
V_2	64HP
V_3	1181
IC 35 PIN 7 = IC 15 PIN 6	P255

Test point TP	Signature
ROMØ	4POA
ROM1	12U3
ROM2	PC01
ROM3	F2A6
ROM4	6H49
ROM5	0996
ROM6	U3H5

Test point TP	Signature
ROMØØ	755U
ROMØ1	0001
ROMØ2	0001
ROMØ3	0001
ROMØ4	0001

Test point TP	Signature
RAMØ	PF2P
RAM1	8F14
RAM2	U81U
RAM3**	3UP7
IC 36 PIN 7	7A71

Decodet addresses

Notes

START: ⌝ TP ROMØ

STOP: ⌝ TP ROMØ

CLOCK: ⌟ TP OE (ALE, connector Pin C12, ⌝)*

GROUND: TP M

Stimulus: Free-running

Frame signature: 0001

Fig. 6.12-8 Address signatures (CPU board)

* ADØ, AD6 and AD7: only valid when measured directly on the microprocessor pins.

** Only applicable if the arithmetic processor is installed

6.12.3.3 Troubleshooting in the event of a RAM fault

If a RAM fault occurs, address lines AØ to A7 should first be checked using signature analysis. Subsequently check the signatures at the chip enable inputs of the RAMs. Refer to the Section on "Address signatures".

Once this has been done, the data lines can be checked (see Fig. 6.12-9).

Test point	Signature	Remarks
The signature on lines DØ...D7 must be the same as the signatures on lines ADØ...AD7. (As the signature is dependent on the RAM contents, a check can only be made here as to whether the signature is identical over the entire signal path.)		↘ START: TP RAMØ...3 ↗ STOP: TP same as START ↗ CLOCK: TP OE Stimulus: Free-running

Fig. 6.12-9 RAM signatures (data lines)

6.13 TROUBLESHOOTING THE IEEE 488/<IEC 625> INTERFACE BUS CARD BN 958, CIRCUIT DIAGRAM (91)

6.13.1 INTRODUCTION

The bus interface BN 958 is used to adapt microprocessor-controlled instruments to the IEEE 488 or <IEC 625> interface bus.

For the purposes of this test, it is assumed that the device is operating correctly as regards the program sequence and control of the device- to-IEC 625-interface.

Since the card cannot be tested completely when fitted in the instrument, it is advisable to replace it in the event of a fault.

6.13.2 EXTRA DEVICE-SPECIFIC TEST

IEC bus interface card test

The signal path (address bus, data bus, control bus) to the IEC bus module is checked in relation to the gate address.

The bus interface card is optional. It is not possible to use a software routine to check whether it is fitted or not should the instrument not respond to IEC bus commands, since no signal line is provided for this purpose.

S 1/	1	2	3	4	5	6	7	8	9	10
ON				•	•	•	•	•		•
OFF	•	•	•						•	

cyclic IEC bus test

Fig. 6.13-1 DIL switch settings for IEC bus test

Calling up the test:

Set DIL switch S 1 on the connected CPU-2 (2A) as shown above and switch on the instrument.

Test result:

Connect an oscilloscope to TP 2 (SOD) of the CPU card:

Frequency = Ø -> Faulty

Frequency ≠ Ø -> OK

6.14 TROUBLESHOOTING IN THE POWER SUPPLY UNIT

- Transformer unit
- Wiring card
- -5.2 V linear controller
- Charging circuit
- Control unit
- DC/DC converter

Auxiliary equipment: - 1 Auxiliary load (see Section 5.11, Power supply unit)
- 1 Variable ratio transformer
- 2 AC/DC multimeters
- 1 Oscilloscope with test probe

6.14.1 TRANSFORMER UNIT

No special data necessary for troubleshooting.
No alignment necessary.
No DC/DC converter necessary.

6.14.2 WIRING CARD

After checking the voltage of the fuses, only visual inspection (for burns) can be carried out here. On these 6-layer boards, repairs can only be performed by repairing a conductor with cable.
The solder-in fuses should be cut off, not desoldered, for replacement. The new fuses are then soldered onto the remaining ends.
From Series B onwards, fuses Si 2 ... 5 are normal fuses in holders.

6.14.3 -5.2 V LINEAR CONTROLLER

The +12 V, -12 V, +5 V converters can be removed.

Series A: Small board on the rear of the wiring card
Series B: Linear controller located on the charging circuit board

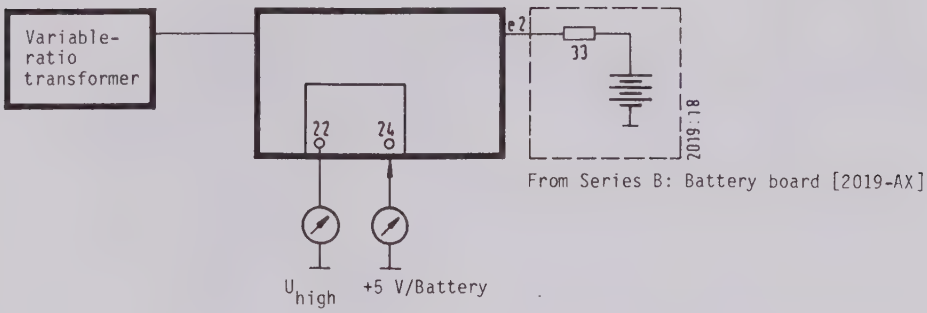
The check can be made in the power supply unit. At a mains voltage of 220 V, -6.3 V should be present at Pt. 34 -> 36 .

Check the voltages at power transistor T 7.
E: -6.3 V
C: -5.25 V
Pt.: 37 -> 36⊥: -5.25 V

6.14.4 CHARGING CIRCUIT

The +12 V, -12 V, -6.3 V converters can be removed.
The measurement should be performed in the instrument.

Test setup:



Switching threshold check

220 V variable-ratio transformer Check the high-end voltage at Pt. 22: +30 V-
Check the +5 V at Pt. 23 : +5.0 V ± 0.1 V

Use a 100 kΩ/V instrument to measure the voltage at Pt. 24: +5.0 V.
Turn down the mains voltage on the variable-ratio transformer; observe the high-end voltage at Pt. 22 and the DR voltage at Pt. 24.
When reaching U_{ob} = 17.5 V ± 0.2 V, T 2 switches from +5 V voltage to 3.5...4 V storage battery voltage.
Turn up the mains voltage. At a high-end voltage of 19 V ± 0.2 V, T 2 should again switch from the battery to +5 V.

Charging current check

Mains voltage 220 V, high-end voltage +30 V-
Series A: Measure the charging current by disconnecting a storage battery -> contact with a Perlinax disk.
Use a 100 kΩ/V instrument to measure the current: 8...10 mA.

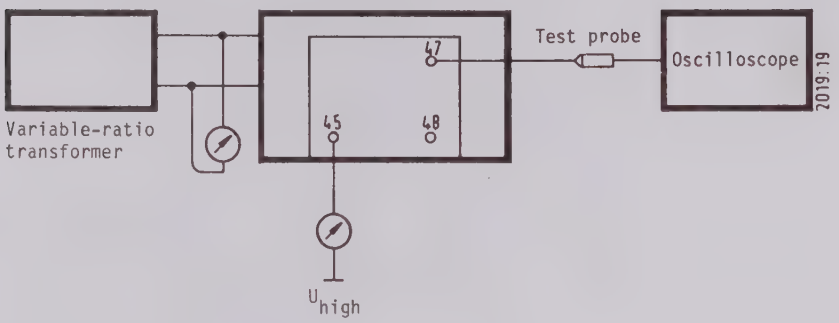
From Series B*: Connect the battery board at socket e2,
measure the charging current in the line to the battery board or at Pt. 25: 8...10 mA.

* Only valid with auxiliary load (see Section 5.11, Fig. 5.11-1).
Check with instrument as under Series A.

6.14.5 CONTROL UNIT

No DC/DC converters are required.
Measurement and alignment can be performed in the power supply unit.

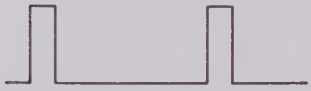
Test setup:



With 220 V mains high-end voltage, check at Pt. 45: +30 V

Sync. voltage

Mains voltage 220 V
Connect oscilloscope with test probe at Pt. 47.
Oscilloscope: AC 0.1 V/an 0.5 µs/an
Measure the pulse voltage:



Pulse height : 5 ... 6 V_{pp}
Pulse width : 300 ns ± 100 ns
Pulse interval: 24.7 µs ± 0.2 µs

The pulse interval can also be measured with a counter and 1 MHz test probe: 405 kHz

Also check the sync. voltage at the inputs of the DC/DC converters.
Pt.: a C, b C, d C, c C

Data-save signal

Test setup as above, without oscilloscope
Slowly increase the mains voltage, observing the data-save signal at Pt. 48. Measure the high-end voltage.
The DR voltage rises to 2.5 ... 5 V, jumping back to < 0.8 V at a mains voltage of approx. 140 V.
Required high-end voltage: 19 V ± 0.2 V
Turn down the mains voltage again until the DR signal re-appears. Required high-end voltage: 16.5 V ± 0.5 V.
Also check the signal at Pt. e 15.

6.14.6 DC/DC MODULES

For a simple functional check or troubleshooting in the DC/DC converters, connect the unit under test in accordance with Fig. 6.14-1.

Test setup:

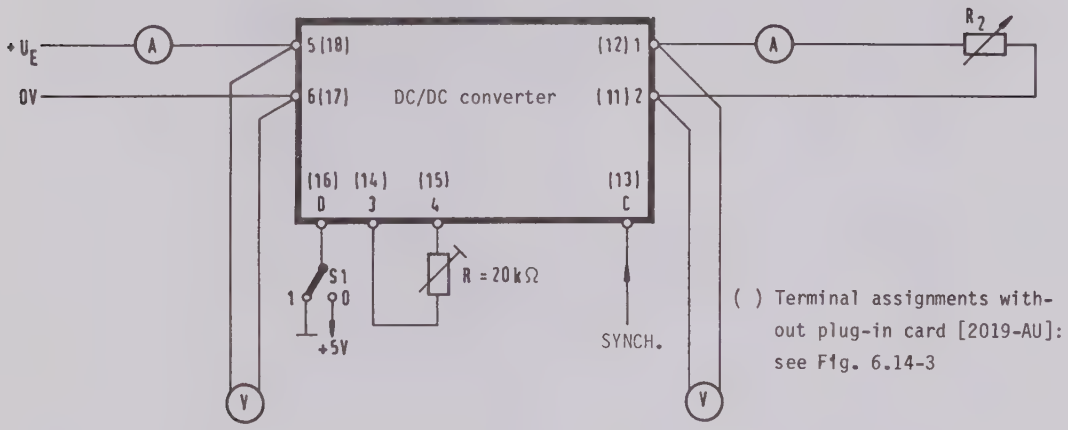


Fig. 6.14-1 Functional check of the DC/DC converters

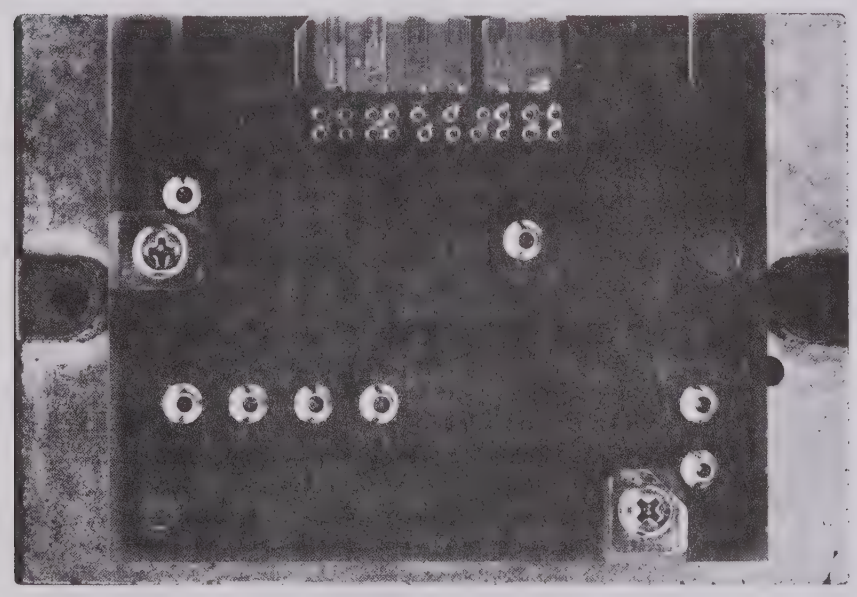


Fig. 6.14-2 Terminal assignments with plug-in card [2019-AU]

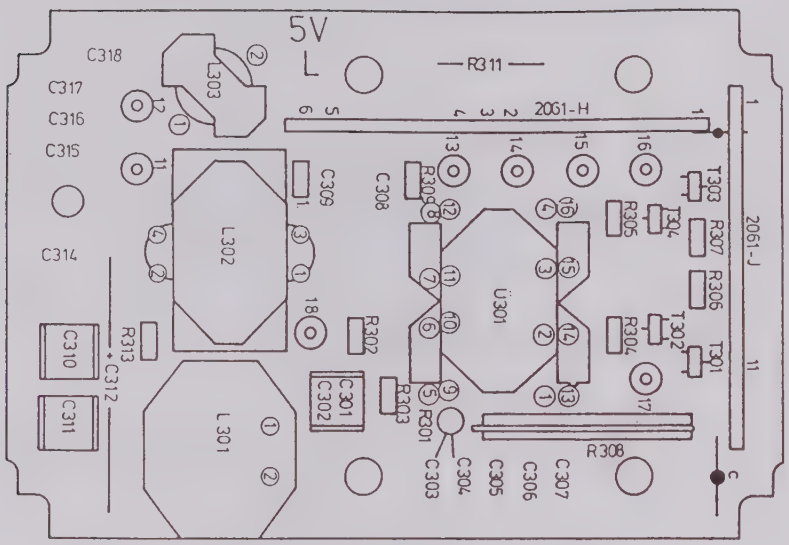


Fig. 6.14-3 Terminal assignments without plug-in card [2019-AU]

Functional check

Measurement 1: Set S 1 to position 1

U_E = 24 V; I_A = 0
Terminal C not assigned

Measurement: I_E = 0,01 ... 0,3 A
U_A = $U_{A\ NOM}$ ± 10%

Measurement 2: I_A = $I_{A\ NOM}$

Measurement: I_E = 1 ... 1.9 A
U_A = $U_{A\ NOM}$ ± 10%

Measurement 3: Set S 1 to position 0

Measurement: U_A = -0.100 ... -0.1 V

Measurement 4: Set S 1 to position 1

Measurement: Frequency at terminal 10
230 kHz ... 295 kHz

Measurement 5: Apply external sync. frequency at terminal C, as per Fig. 6.13-1.

Measurement 6: Use R 1 to set output voltage U_A to $U_{A\ NOM}$ ± 0.2%

Measurement: R 1 = 7.4 kΩ ... 11.8 kΩ

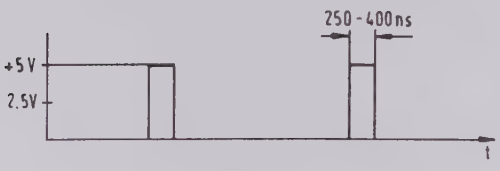
Measurement 7: U_E = 17 ... 40 V
I_A = $I_{A\ NOM}$

Measurement: U_A = $U_{A\ NOM}$ ± 1%

Measurement 8: U_E = 24 V

$I_A = I_{A\ NOM}/6$

Measurement: $U_A = U_{A\ NOM} \pm 1\%$



f = 430 kHz

Fig. 6.14-4 Synchronization signal

7 ALIGNMENT INSTRUCTIONS 7-1

7.1 Alignment summaries 7-1
7.1.1 List of all alignments 7-1
7.1.2 Alignment work after replacement/alignment of boards 7-4
7.1.3 Alignment work after replacement of assemblies 7-6
7.1.4 General notes on alignment 7-7

7.2.1 Frequency generator (A) 7-7
7.2.1.1 Carrier oscillator alignment 7-7
7.2.1.1.1 +9 V alignment (5 P 1) 7-7
7.2.1.1.2 Amplitude (5 P 2) 7-7
7.2.1.2 Carrier phase meter alignment 7-7
7.2.1.2.1 Offset (6 P 1) 7-7
7.2.1.2.2 44 MHz peak (6 C 24) (from Series C onwards) 7-8
7.2.1.3 Lock-in oscillator alignment 7-8
7.2.1.3.1 Centre frequency, resonant circuit (6 0 101) 7-8
7.2.1.3.2 Tuning voltage (6 P 100... and 6 R 135...) 7-9
7.2.2 Input circuit (B) 7-10
7.2.2.1 Input circuit frequency response (2 C 59) 7-10
7.2.2.2 Frequency response in equalizer mode (2 C 22) 7-10
7.2.2.3 Absolute equalizer level (2 P 1) 7-11
7.2.2.4 Equalizer reference (2 P 2) 7-11
7.2.2.5 Threshold alignment (2 P 3 ... 2 P 5) 7-12
7.2.3 Code error (C) 7-13
7.2.3.1 Code error 1 alignment 7-13
7.2.3.1.1 Clock symmetry alignment (3 P 3) 7-13
7.2.3.1.2 DA^+ symmetry alignment (3 P 1) 7-13
7.2.3.1.3 Da^- symmetry alignment (3 P 2) 7-14
7.2.3.1.4 Basic phase alignment (7 C 106) 7-16
7.2.3.1.5 Basic delay alignment (3 bridge A...K) 7-16
7.2.3.1.6 Bit rate-dependent delay alignment (3 P 5 ... 3 P 8) 7-16
7.2.3.1.7 Note on functional check 7-17
7.2.3.2 Code error 2 alignment 7-17
7.2.4 220 MHz circuit (D) 7-18
7.2.4.1 220 MHz VCO alignment 7-18
7.2.4.1.1 Frequency (7 C 19) 7-18
7.2.4.1.2 Amplitude (7 P 1) 7-18
7.2.4.2 Controller 2 alignment (7 R 415) 7-19
7.2.4.3 Sawtooth phase meter alignment 7-19
7.2.4.3.1 Switching threshold (7 P 301) 7-19
7.2.4.3.2 Symmetry (7 C 327) 7-19
7.2.4.3.3 Reference voltage (7 P 302) 7-20
7.2.4.4 Mixer alignment 7-21
7.2.4.4.1 90° phase (7 C 106) 7-21
7.2.4.4.2 440 MHz wave trap (7 C 111) 7-22
7.2.5 11 MHz circuit (E) 7-22
7.2.5.1 11 MHz phase meter alignment (8 P 2) 7-22
7.2.5.2 20:1 divider (8 C 106) 7-22
7.2.5.3 11 MHz filter (8 L 201, 8 L 202) 7-22
7.2.5.4 Controller 1 alignment 7-22
7.2.5.4.1 Gain (9 P 2) (2 Hz alignment) 7-23
7.2.5.4.2 11 MHz frequency (9 P 3) 7-23
7.2.5.4.3 Lock-in aid (9 P 1) 7-23
7.2.6 Adder (F) 7-25
7.2.6.1 General information 7-25
7.2.6.2 11 MHz path gain (10 P 101) 7-27
7.2.6.3 220 MHz path gain (10 P 102) 7-28
7.2.6.4 Slope of the sawtooth phase meter for 2048 kbit/s 7-29
7.2.6.5 Current source zero point (10 P 10, P 11) 7-30
7.2.6.6 Frequency response compensation (10 C 128, C 108) 7-31
7.2.6.7 LP filter cutoff frequency (10 C 104) 7-31
7.2.6.8 Delay correction (10 S 1 ... S 4) 7-32
7.2.7 Filter (H) 7-33
7.2.7.1 Demodulator output slope (11 P 2) 7-33
7.2.7.2 Demodulator output frequency response (11 C 37) 7-33
7.2.8 Peak rectifier (K) 7-34
7.2.8.1 30 dB amplifier gain (12 P 1) 7-34
7.2.8.2 Offset alignment (12 P 4, 12 P 5) 7-35
7.2.8.3 Peak value meter gain (12 P 2, P 3) 7-35
7.2.8.4 Frequency response alignment (12 C 405, C 205) 7-36
7.2.8.5 Hit counter frequency response (12 C 305) 7-37

7.2.9 Hit counter (I) 7-37
7.2.9.1 Gain (13 P 1) and offset (13 P 2, 13 P 3) 7-37
7.2.9.2 Real-time clock (13 C 6) 7-39
7.2.10 RF control 7-39
7.2.10.1 Charging current $I_{\varphi s}$ (14 P 2) 7-39
7.2.10.2 Current source DAC offset (14 P 1) 7-39
7.2.10.3 -5.2 V setting (14 P 3) 7-39
7.2.10.4 Equalizer amplifier alignment (14 P 5, P 6, P 7) 7-39
7.2.11 Power supply unit (N) 7-40
7.2.11.1 Complete power supply unit 7-40
7.2.11.2 DC/DC modules 7-40
7.2.11.3 -5.2 V linear controller 7-40
7.2.11.4 Charging circuit 7-40
7.2.11.5 Control unit 7-41
7.2.11.6 Data-save signal 7-42

7 ALIGNMENT INSTRUCTIONS

7.1 ALIGNMENT SUMMARIES

7.1.1 LIST OF ALL ALIGNMENTS

Assembly/ circuit	Alignment element	Function	Section
Frequency generator (A)			7.2.1
Carrier oscillator [2019-P]	5 P 1	+9 V alignment	7.2.1.1.1
	5 P 2	Amplitude	7.2.1.1.2
Carrier phase meter [2019-Q]	6 P 1	Offset	7.2.1.2.1
	6 C 24	44 MHz peak (from Series C onwards)	7.2.1.2.2
Lock-in oscillator [2019-R]	6 O 101	Centre frequency, resonant circuit	7.2.1.3.1
	6 P 100 ... 109	Tuning voltage	7.2.1.3.2
	6 R 135 ... 144	Tuning voltage, alignment values	7.2.1.3.2
Input circuit (B) [2019-V]			7.2.2
	2 P 1	Absolute equalizer level	7.2.2.3
	2 P 2	Equalizer reference	7.2.2.4
	2 P 3	+ threshold	7.2.2.5
	2 P 4	0 threshold	7.2.2.5
	2 P 5	- threshold	7.2.2.5
	2 C 22	Frequency response, input circuit	7.2.2.1
	2 C 59	Frequency response, equalizer mode	7.2.2.2
Code error (C)			7.2.3
Code error 1 [2019-AL]	3 P 1	Data (+) symmetry	7.2.3.1.2
	3 P 2	Data (-) symmetry	7.2.3.1.3
	3 P 3	Clock symmetry	7.2.3.1.1
	3 P 5	Delay setting: 0.7 ... 55 MHz	7.2.3.1.6
	3 P 6	55 ... 105 MHz	7.2.3.1.6
	3 P 7	105 ... 145 MHz	7.2.3.1.6
	3 P 8	145 ... 168 MHz	7.2.3.1.6
	3 bridge A...K	Basic delay	7.2.3.1.5
Code error 2 [2019-AO]	4 P 1	Signal symmetry	7.2.3.2

Fig. 7.1.1-1 Alignment elements

Assembly/ circuit	Alignment element	Function	Section
220 MHz circuit (D)			7.2.4
220 MHz VCO [2019-M]	7 C 19	Frequency	7.2.4.1.1
	7 P 1	Amplitude	7.2.4.1.2
Controller 2 [2019-N]	10 R 415	Gain (alignment value)	7.2.4.2
Sawtooth phase meter [2019-O]	7 P 301	Switching threshold	7.2.4.3.1
	7 C 327	Symmetry	7.2.4.3.2
	7 P 302	Reference voltage	7.2.4.3.3
Mixer [2019-U]	7 C 106	90° phase	7.2.4.4.1
	7 C 111	440 MHz wave trap	7.2.4.4.2
11 MHz circuit (E)			7.2.5
11 MHz phase meter [2019-G]	8 P 2	Linearity	7.2.5.1
20:1 divider [2019-AM]	8 C 106	220 MHz peak	7.2.5.2
11 MHz filter [2019-AN]	8 L 201	22 MHz peak	7.2.5.3
	8 L 202	11 MHz peak	7.2.5.3
Controller 1 [2019-H]	9 P 1	Lock-in aid	7.2.5.4.3
	9 P 2	Gain	7.2.5.4.1
	9 P 3	11 MHz frequency	7.2.5.4.2
Adder (F) [2019-AF]			7.2.6
	10 P 101	Gain, 11 MHz path	7.2.6.2
	10 P 102	Gain, 220 MHz path	7.2.6.3
	10 P 10	Current source neutral point	7.2.6.5
	10 P 11	Current source neutral point	7.2.6.5
	10 C 104	Low-pass filter cutoff frequency	7.2.6.7
	10 C 128	Frequency response compensation	7.2.6.6
	10 C 108	Frequency response compensation	7.2.6.6
	10 S 1	Delay correction	7.2.6.8
	...S 4		
Filter (H) [2019-Y]			7.2.7
	11 P 2	Demodulator output slope	7.2.7.1
	11 C 37	Demodulator output frequency response	7.2.7.2

Fig. 7.1.1-1 Alignment elements (contd.)

Assembly/ circuit	Alignment element	Function	Section
Rectifier (K) [2019-Z]			7.2.8
	12 P 1	30 dB amplifier gain	7.2.8.1
	12 P 2	Gain -ū	7.2.8.3
	12 P 3	Gain +ū	7.2.8.3
	12 P 4	Offset -ū	7.2.8.2
	12 P 5	Offset +ū	7.2.8.2
	12 C 205	Frequency response, 30 dB amplifier	7.2.8.4
	12 C 305	Frequency response, hit counter amplifier	7.2.8.5
	12 C 405	Frequency response, peak rectifier	7.2.8.4
Hit counter (I) [2019-AA]			7.2.9
	13 P 1	Hit counter gain	7.2.9.1
	13 P 2	Hit counter threshold + offset	7.2.9.1
	13 P 3	Hit counter threshold - offset	7.2.9.1
	13 C 6	Real-time clock	7.2.9.2
RF control (G) [2019-F]			7.2.10
	14 P 1	Current source DAC offset	7.2.10.2
	14 P 2	Charging current	7.2.10.1
	14 P 3	-5.2 V setting	7.2.10.3
	14 P 5	Equalizer amplifier offset	7.2.10.4
	14 P 6	Equalizer amplifier gain	7.2.10.4
	14 P 7	Equalizer amplifier frequency response	7.2.10.4

Fig. 7.1.1-1 Alignment elements (contd.)

7.1.2 ALIGNMENT WORK AFTER REPLACEMENT/ALIGNMENT OF BOARDS

Replaced circuit	Alignment operation	After replacement of the circuit, check: Further circuitry	Alignment element	After alignment of ..., check Alignment element	Section
Carrier osc. [2019-P] (5)	Pre-align	-/-			
Carrier phase meter [2019-Q] (6)	Instrument alignment 7.2.1.2	-/-			
Lock-in osc. [2019-R] (6)	Pre-align	-/-			
Input circuit [2019-V] (2)	Pre-align	Code error [2019-AL]	3 P 1 3 P 2		7.2.3.1.2 7.2.3.1.3
Code error 1 [2019-AL] (3)	Instrument alignment 7.2.3.1	-/-			
Code error 2 [2019-AO] (3)	Instrument alignment 7.2.3.2	-/-			
220 MHz VCO [2019-M] (7)	Pre-align	Contr. 2 [2019-M]	10 R 415		7.2.4.2
Controller 2 [2019-N] (7)	Instrument alignment 7.2.4.2	-/-			
Sawtooth phase meter [2019-O] (7)	Instrument alignment 7.2.4.3	Adder [2019-AF]	10 P 102 10 C 128 10 C 108		7.2.6.3 7.2.6.6 7.2.6.6
		Mixer [2019-U]	7 C 106	7 P 302 7 C 327	7.2.4.4.1
		Code error 1 [2019-AL]	3 P 5 3 P 6 3 P 7 3 P 8 3 bridge A...K	7 C 327	7.2.3.1.6 7.2.3.1.6 7.2.3.1.6 7.2.3.1.6 7.2.3.1.5
		RF control [2019-F]	14 P 1		
Mixer [2019-U] (7)	Instrument alignment 7.2.4.4	Code error [2019-AL]	3 bridge A...K 3 P 5...8		7.2.3.1.5 7.2.3.1.6

Fig. 7.1.2-1 Alignment work after replacement/alignment of boards

Replaced circuit	Alignment operation	After replacement of the circuit, check: Further circuitry	Alignment element	After alignment of ..., check Alignment element	Section
170 MHz LP 0° [2019-T] (7)	-/-	Code error [2019-AL]	3 bridge A...K		7.2.3.1.5
170 MHz LP 90° [2019-T] (7)			3 P 5...8		7.2.3.1.6
11 MHz phase meter [2019-G] (8)	Factory alignment ONLY	Adder [2019-AF]	10 P 101 10 P 102 10 C 104	8 P 2	7.2.6.2 7.2.6.3 7.2.6.7
11 MHz VCO [2019-J] (8)	-/-	Controller 1 [2019-H]	9 P 2 9 P 3		7.2.5.4.1 7.2.5.4.2
20:1 divider [2019-AM] (8)	Instrument alignment 7.2.5.2	-/-			
11 MHz filter [2019-AN] (8)	Pre-align	-/-			
Controller 1 [2019-H] (8)	Instrument alignment 7.2.5.4	-/-			
Adder [2019-AF] (10)	Instrument alignment 7.2.6	-/-			
As a rule, both circuits are replaced as a single, completely tested unit.					
Filter [2019-Y] (11)	7.2.7	Hit counter [2019-AA]	13 P 1		7.2.9.1
Rectifier [2019-Z] (12)	7.2.8		13 P 2 13 P 3		7.2.9.1 7.2.9.1
Hit counter [2019-AA] (13)	Instrument alignment 7.2.9	-/-			
RF control [2019-F] (14)	Instrument alignment 7.2.10	Adder [2019-AF]	10 P 102	14 P 2	7.2.6.3
DC/DC modules	-/-	-/-			

Fig. 7.1.2-1 Alignment work after replacement/alignment of boards (contd.)

7.1.3 ALIGNMENT WORK AFTER REPLACEMENT OF ASSEMBLIES

Assembly	After replacement of the assembly, check: Circuit	Alignment element	Section
Frequency generator (A), complete, consisting of:			
- Lock-in oscillator	Mixer	7 C 106	7.2.4.4.1
- Carrier phase meter	[2019-U]		
- Carrier oscillator			
- Mixer	Code error 1	3 P 5	7.2.3.1.6
- 170 MHz LP 0°	[2019-AL]	3 P 6	7.2.3.1.6
		3 P 7	7.2.3.1.6
		3 P 8	7.2.3.1.6
		3 bridge A...K	7.2.3.1.5
Frequency generator (A), complete, but not replaced:			
- Mixer	No further instrument alignment		7.2.3
- 170 MHz LP 0°			
RF chassis, complete, consisting of:			
- Frequency generator (A)	Code error 1	3 P 5	7.2.3.1.6
- Input circuit (B)	[2019-AL]	3 P 6	7.2.3.1.6
- 220 MHz circuit (D)		3 P 7	7.2.3.1.6
- 11 MHz circuit (E)		3 P 8	7.2.3.1.6
- Adder (F)		3 bridge A...K	7.2.3.1.5
- RF control (G)		3 P 1	7.2.3.1.2
		3 P 2	7.2.3.1.3
RF chassis, complete, additionally replaced:	No further instrument alignment		
- Code error card			
Display/control section (L)	No further instrument alignment		
Power supply unit (N)	No further instrument alignment		

Fig. 7.1.3-1 Alignment work after replacement of assemblies

7.1.4 GENERAL NOTES ON ALIGNMENT

The sequence for circuit alignment is defined by the Section numbers and should be observed without fail.

Various alignments, some on different boards, mutually affect each other. Consequently, alignment work on other circuits may be prescribed within a Section.

7.2.1 FREQUENCY GENERATOR (A)

7.2.1.1 Carrier oscillator alignment

7.2.1.1.1 +9 V alignment (5 P 1)

Alignment: - DVM at 5 IC 1, Pin 2
Use 5 P 1 to set: +9 V ± 0.1 V

7.2.1.1.2 Amplitude (5 P 2)

Instruments: - TEK 495A analyzer with P6201 active test probe

Settings: - Set the lowest built-in bit rate frequency on the PJM-4:
Carrier frequency = 220 MHz + bit rate frequency

Alignment: - Connect the analyzer with active test probe to output 1 (5 Pt. 16) in the carrier oscillator:
Use 5 P 2 to set: Level = -2 dBm

Check:
1. Control voltage:
Connect the DVM to collector 5 T 3 (control voltage) and set all bit rate frequencies consecutively:
The control voltage should always be > -9.5 V.
If not:
Use 5 P 2 to reduce the level slightly.
2. Check the level at outputs 1 (5 Pt. 16) and 2 (5 Pt. 20) at all bit rate frequencies:
-5 dBm < P < +2 dBm

7.2.1.2 Carrier phase meter alignment

7.2.1.2.1 Offset (6 P 1)

Test setup:

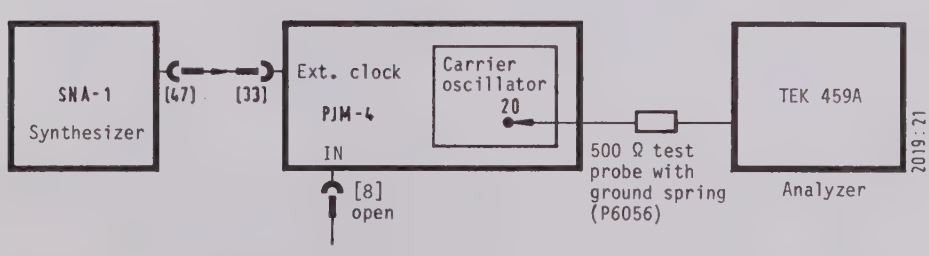


Fig. 7.2.1-1 Sideband noise alignment

Instrument settings:	PJM-4	Bit rate EXTERNAL
	Synthesizer	8.4 MHz, 0 dBm
	Analyzer	F_{cent} = 228.4 MHz F_{span} = 10 kHz BW = 1 kHz SWEEP = 10 ms Ref. = -10 dBm
Alignment:		Use 6 P 1 to align to minimum sideband noise

7.2.1.2.2 44 MHz peak (6 C 24) (from Series C onwards)

Test setup:

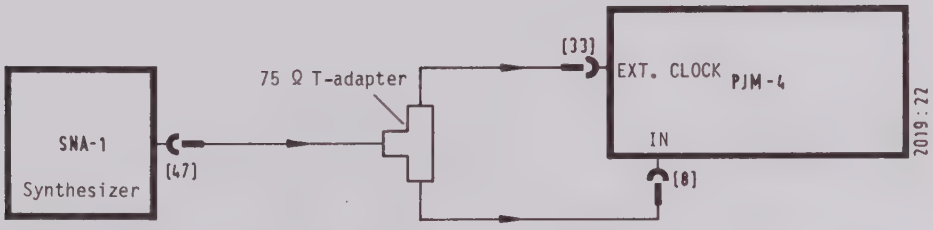


Fig. 7.2.1-2 Alignment for minimizing the inherent jitter display

Instrument settings:	PJM-4	Bit rate EXTERNAL HP = 10 Hz, LP = 600 kHz
	Synthesizer	110.02 MHz, 0 dBm
Alignment:		Use 6 C 24 to minimize the inherent jitter display: Digital value < 30 mUI_{pp}

7.2.1.3 Lock-in oscillator alignment

7.2.1.3.1 Centre frequency, resonant circuit (6 O 101)

Note:	- The alignment is very sensitive - Necessitates re-alignment of trimmers 6 P 100 to 6 P ... for all bit rates fitted
Test setup:	- Connect the DVM between 6 TP 10 (+) and 6 TP 11 (-)
PJM-4 setting:	- Highest built-in bit rate frequency
Alignment:	- Only when entire board aligned: Turn the trimmer 6 P 1... associated with the highest bit rate frequency to its centre position. - Use tuning slug 6 O 101 to maximize the voltage: approx. 0.3 ... 0.6 V

Other necessary alignments:
After aligning 6 O 101, the tuning voltages for all bit rate frequencies must be aligned in accordance with Section 7.2.1.3.2.

7.2.1.3.2 Tuning voltage (6 P 100... and 6 R 135...)

Test setup: - Connect the DVM between 6 TP 10 (+) and 6 TP 11 (-).

PJM-4 settings: - Set the bit rate frequency to be aligned.

Alignment: When installing a new bit rate crystal, align as per Item 1; for re-alignment, carry out the alignment as per Item 6:

1. Use Fig. 7.2.1-3 to determine the trimmer 6 P 1... associated with the crystal and install it.
   6 P 1... is supplied when the option is retrofitted.
2. Set the trimmer to its middle position.
3. Remove the related resistor 6 R 1... (alignment value) and instead connect an external potentiometer or decade resistance as R_{ext}.
   The approximate value for R_{ext} is shown in Fig. 7.2.1-3:
   $R_{ext} \approx R_{tot} - R_{trimmer/2}$
4. Maximize the display on the DVM using R_{ext}.
5. Measure R_{ext} and fit the nearest value from the E-96 series.
6. Again maximize the display with trimmer 6 P 1...; if necessary, vary 6 R 1... if the maximum is not clearly exceeded with 6 P 1....

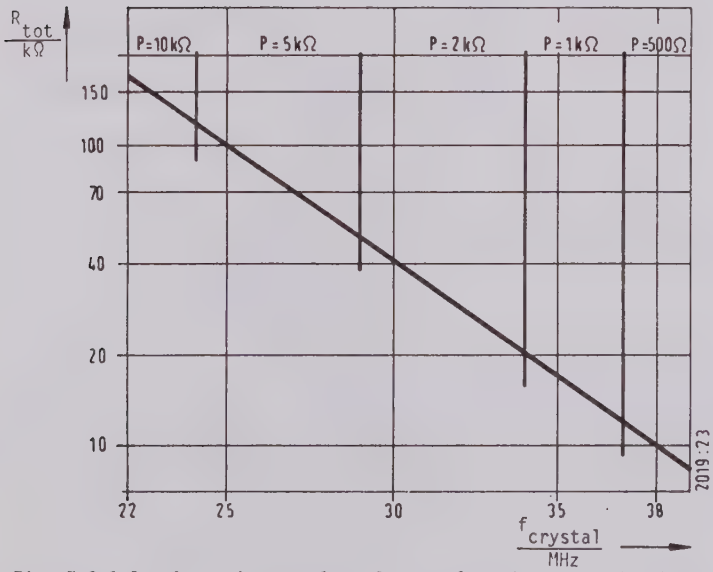


Fig. 7.2.1-3 Approximate values for total resistance and trimmer P

7.2.2 INPUT CIRCUIT (B)

7.2.2.1 Input circuit frequency response (2 C 59)

Instruments: Level measuring setup SPM/PSS-16 with display or spectrum and network analyzer SNA-1/02

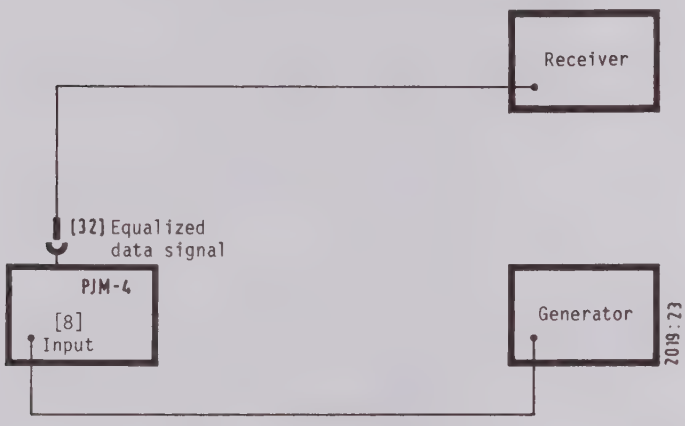


Fig. 7.2.2-1 Test setup for aligment of the input circuit frequency response

Settings:

PJM-4	Code: CMI	
	EQU: FLAT	
Level. measuring setup	Sweep	
	Start frequency	1 MHz
	Stop frequency	160 MHz
	Send level	-15 dBm

Alignment: Use 2 C 59 to align the frequency reponse to minimum slope.
The frequency response, incl. ripple, must be < 1.5 dB.

The short-circuit frequency response of the test setup must be considered.

7.2.2.2 Frequency response in equalizer mode (2 C 22)

Instruments and test setup as in Section 7.2.2.1.
Connect a coaxial cable (Type RG 59B/U) of 124 m length (= 12 dB attenuation at 70 MHz) between generator and PJM-4, or insert test device 2-2019.*
Remove bridge A-B in input circuit (2) and apply +10.0 V to Pt. A.

Alignment: Use 2 C 22 to align to minimum slope.
Required frequency response in the range 20 ... 150 MHz $\leq$ 3.0 dB.

* If the cable is not available, replace the "Input circuit (2)" board with an aligned one.

7.2.2.3 Absolute equalizer level (2 P 1)

Instruments and test setup as in Section 7.2.2.1.
Level measuring setup setting: f = 70 MHz.
Remove bridge A-B in the input circuit (2).
Measure the level at "Equalized data signal" output [32].

Reduce the send level by 12 dB.
Apply +10 V at Pt. A of the input circuit (2).
Use 2 P 1 to set the level at "Equalized data signal" output [32]
to the previously measured value.

7.2.2.4 Equalizer reference (2 P 2)

Test setup: PCM pattern generator PJG-4 or PF-4
Oscilloscope BW > 200 MHz (e.g. TEK 2465)
Matching pad 50/75 Ω

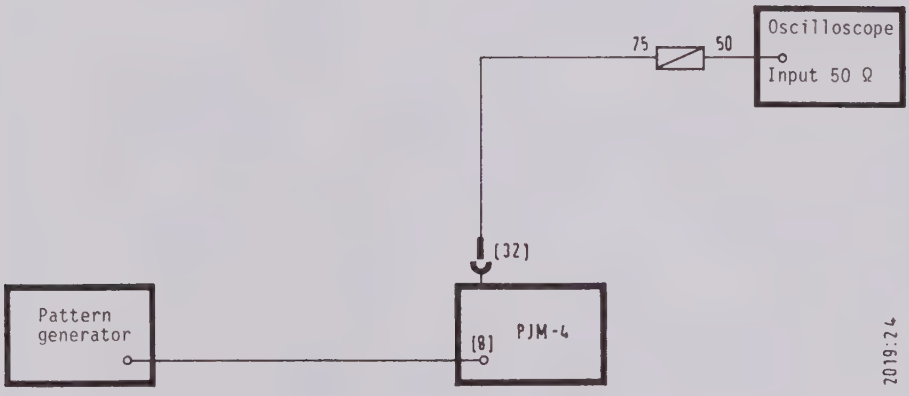


Fig. 7.2.2-2 Test setup for signal amplitude alignment

Pattern generator: 139 Mbit/s, CMI, constant "1" at 1...16

PJM-4 : CMI, 139 Mbit/s, Flat [4]
NOMINAL AMPLITUDE: 0.50 V_p

Measure the signal amplitude at the "Equalized data signal" output. Approximate value 170 mV_p.

Insert a 100 m coax cable (RG 59 B/U)* between pattern generator and PJM-4 einfügen. Switch on $\sqrt{f}$ [4] on the PJM-4.

Use 2 P 2 to set the signal amplitude to the previously measured value.

* If the cable is not available, replace the "Input circuit (2)" board with an aligned one.

7.2.2.5 Threshold alignment (2 P 3 ... 2 P 5)

Instruments: Level generator, f = 10 MHz, 0 dBm, e.g. PS-19
Spectrum analyzer, B = 50 MHz, e.g. SNA-1
Active test probe (TK-11)

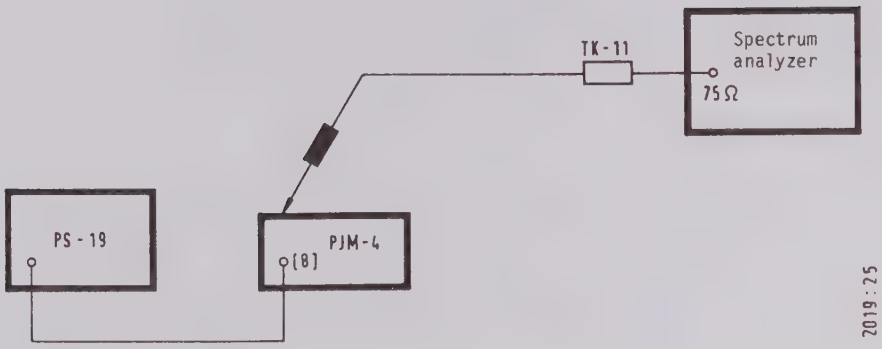


Fig. 7.2.2-3 Test setup for threshold alignment 2 P 3 ... 2 P 5

Use the spectrum analyzer and TK-11 to measure at R 160/C 77 of input circuit [2019-V].

Threshold 0 (2 P 4)

PJM-4: Code CMI, Flat [4], 139 Mbit/s
NOMINAL AMPLITUDE: 0.50 V_p

Use P 4 to align the 20 and 40 MHz spectral lines to a minimum.
Required distance from the 10 MHz spectral line $\geq$ 35 dB.

Threshold + (2 P 3)

PJM-4: Code ECL NRZ, Flat [4], 139 Mbit/s
NOMINAL AMPLITUDE: 0.40 V_p

Use P 3 to align the 20 and 40 MHz spectral lines to a minimum.
Required distance from the 10 MHz spectral line $\geq$ 35 dB.

Threshold - (2 P 5)

PJM-4: Code AMI, Flat [4], 139 Mbit/s
NOMINAL AMPLITUDE: 2.37 V_p

Use P 5 to align the 10 and 30 MHz spectral lines to a minimum.
Required distance from the 20 MHz spectral line $\geq$ 35 dB.

7.2.3 CODE ERROR (C)

7.2.3.1 Code error 1 alignment

7.2.3.1.1 Clock symmetry alignment (3 P 3)

Instruments:

	Oscilloscope	BW ≥ 300 MHz (e.g. TEK 2465)
	Sine-wave generator	f ... 160 MHz (e.g. SNA-1 and PSS-16)
		Level ... +6 dBm
	Power splitter	75 Ω
	Adapter card	AK-3

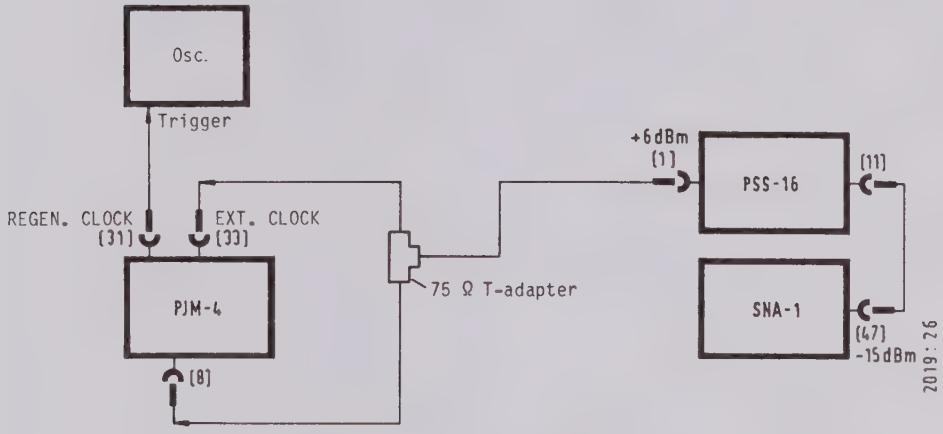


Fig. 7.2.3-1 Test setup for code error card 1 alignment

Settings:

PJM-4	CMI, EXTERNAL
Generator	140 MHz, +6 dBm

Check: With 500 Ω test probe at (3) IC 4/Pin 5, Ground Pin 9. When "EDGE" key [4] is pressed several times, the signal duty cycle must not change.

Alignment: Maky any necessary symmetry alignment with (3) P 3.

7.2.3.1.2 DA^+ symmetry alignment (3 P 1)

Instruments: As in Section 7.2.3.1.1

Test setup: As in Section 7.2.3.1.1

Settings: As in Section 7.2.3.1.1

Check: With 500 Ω test probe at (3) IC 4/Pin 6, Ground Pin 9.
Only display one signal period; the signal must be symmetrical
(tolerance: ± 140 ps ≙ ± 0.2 divisions)

Alignment: If necessary, align with (3) P 1.

7.2.3.1.3 DA⁻ symmetry alignment (3 P 2)

This is only necessary if a new alignment was also performed under Section 7.2.3.1.2.

Relocate the cable from ST 1 to ST 3 on wiring card [2019-D] (see Fig. 7.2.3-2).

Instruments: As in Section 7.2.3.1.1

Test setup: As in Section 7.2.3.1.1

Settings: As in Section 7.2.3.1.1

Check: With 500 Ω test probe at (3) IC 4/Pin 24, Ground Pin 9 of IC 3. Only display one signal period; the signal must be symmetrical (tolerance: ± 140 ps ≅ ± 0.2 divisions).

Alignment: If necessary, align with (3) P 2.

Important: After the alignment, return the cables to their original positions.

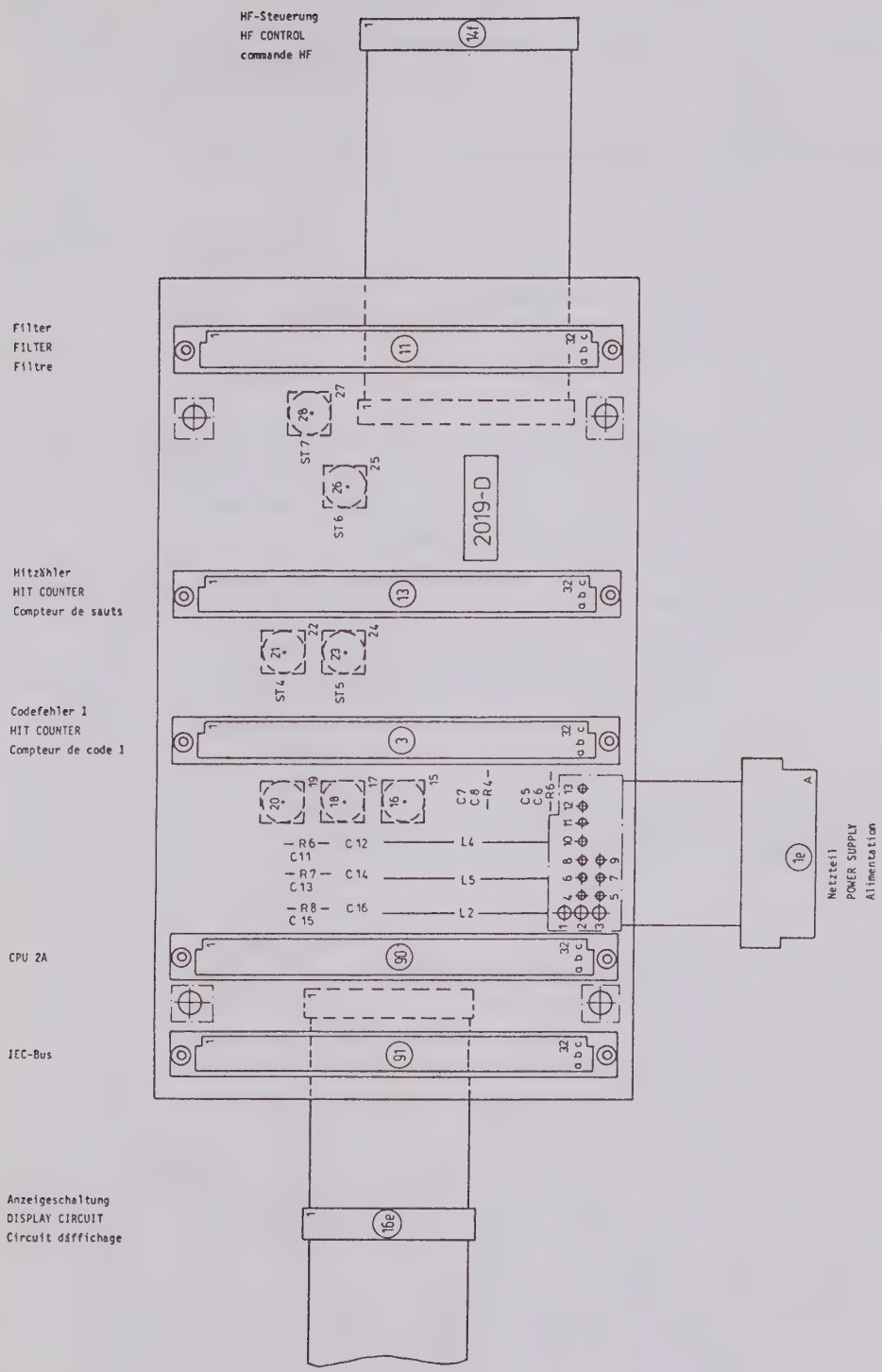


Fig. 7.2.3-2 Signal diagram (20)

7.2.3.1.4 Basic phase alignment (7 C 106)

Instruments, test setup, settings and alignment as in Section 7.2.4.4 (Mixer alignment).

7.2.3.1.5 Basic delay alignment (3 bridge A...K)

Instruments: As in Section 7.2.3.1

Test setup: As in Section 7.2.3.1

Settings:
PJM-4 CMI; EXTERNAL
Generator 160 MHz; +6 dBm
Oscilloscope External trigger

Check:
With test probe at (3) IC 4, Pin 6.
Display one signal period; falling edge at left hand side of screen.
Same test probe at (3) IC 4, Pin 5. The rising edge must lag 90° behind the falling edge of the other signal (≙ 2.5 divisions).
Tolerance: ± 7.5° ≙ ± 0.2 divisions.

Alignment:
Should alignment be necessary, first set (3) P 8 to its middle position; if the rising edge is then within the tolerance of ± 15° ≙ ± 0.4 divisions, only the bit rate-dependent delay correction need be re-aligned (Section 7.2.3.1.6). If not, the bridge on delay correction circuit [2019-AR] must be removed and the necessary replacement determined.

7.2.3.1.6 Bit rate-dependent delay alignment (3 P 5 ... 3 P 8)

Instruments: As in Section 7.2.3.1

Test setup: As in Section 7.2.3.1

Delay alignment, 145 Mbit/s - 168 Mbit/s (3 P 8)

Settings:
PJM-4 CMI; EXTERNAL
Generator 160 MHz, +6 dBm
Oscilloscope External trigger

Check: As in Section 7.2.3.1.5

Alignment:
Should alignment be necessary, use (3) P 8 for alignment. If alignment is impossible, check Sections 7.2.3.1.4 and 7.2.3.1.5.

Delay alignment, 105 Mbit/s - 145 Mbit/s (3 P 7)

Settings:
PJM-4 CMI; EXTERNAL
Generator 140 MHz, +6 dBm
Oscilloscope External trigger

Check: As in Section 7.2.3.1.5

Alignment:
Should alignment be necessary, use (3) P 7 for alignment.

Delay alignment, 55 Mbit/s - 105 Mbit/s (3 P 6)

Settings: PJM-4 CMI; EXTERNAL
Generator 100 MHz; +6 dBm
Oscilloscope External trigger

Check: As in Section 7.2.3.1.5

Alignment: Should alignment be necessary, use (3) P 6 for alignment.

Delay alignment, 0,7 Mbit/s - 55 Mbit/s (3 P 5)

Settings: PJM-4 CMI; EXTERNAL
Generator 41 MHz; +6 dBm

Check: As in Section 7.2.3.1.5

Alignment: Should alignment be necessary, use (3) P 5 for alignment.

7.2.3.1.7 Note on functional check

An intentional functional check of the circuit can only be carried out if it is fitted directly in the instrument or a special adapter card [2019-PM 9A] is used. However, this has no effect on alignment, i.e. an adapter card AK 3 901-C can be used for alignment.

7.2.3.2 Code error 2 alignment

Signal symmetry alignment (4 P 1)

Instruments: DVM

Alignment: Measure the voltage between TP 1 (Ground) and (3) IC 1, Pin 22.
Use (4) P 1 to set the voltage between TP 1 (Ground) and TP 2 (Reference) to the same value.

7.2.4 220 MHz CIRCUIT (D)

7.2.4.1 220 MHz VCO alignment

7.2.4.1.1 Frequency (7 C 19)

Two alignment methods are possible (A and B)

Instruments: A) - Universal frequency counter for 11 MHz (e.g. Philips, PM 6672/421)
B) - Bit rate generator: Bit rate $\geq$ 30 Mbit/s, $\Delta f \leq \pm$ 75 ppm
- Oscilloscope : BW $\geq$ 20 MHz

Settings:
- Open Dip-Fix switch 7 S 401 in Controller 2 and connect control voltage output 7 Pt. 46 to ground.
- Fit the cover on the 220 MHz VCO.

Alignment: A) - Connect the frequency counter in the 20:1 divider at 8 Pt. 3
- Use 7 C 19 to align the display:
11 MHz $\pm$ 5 kHz

B) - Connect the bit rate generator and set the PJM-4 to the bit rate (bit rate frequency $\geq$ 30 Mbit/s).
- Connect the oscilloscope at 7 Pt. 43 ($U_{\varphi 2}$).
- Use 7 C 19 to minimize the frequency of the sawtooth oscillation:
f < 100 kHz

Check:
- Lock the PJM-4 to the bit rate frequenz (frequency error $\leq$ 100 ppm)
- Use the DVM to measure the control voltage at 7 Pt. 46:
Required: U = 0 V $\pm$ 100 mV
- If necessary, correct the setting of 7 C 19.

7.2.4.1.2 Amplitude (7 P 1)

Instruments:
- Oscilloscope, BW $\geq$ 300 MHz (e.g. TEK 2465 A)

Settings:
- As in Section 7.2.4.1.1, but VCO without cover

Alignment:
- Connect the oscilloscope in the 220 MHz VCO with 10:1 test probe at collector 7 T 6 (short ground connection, e.g. ground spring).
- Use 7 P 1 to set the amplitude:
U = 800 mV_{pp} $\pm$ 100 mV_{pp}

Check:
- Check the level at 7 Pt. 3:
U = 400 mV_{pp} $\pm$ 100 mV_{pp}

7.2.4.2 Controller 2 alignment (7 R 415)

Check the control limit frequency of the 220 MHz circuit as per Section 4.7.3.

Alignment: If the test limit values are exceeded, 7 R 415 must be replaced in accordance with the data in Section 4.7.3.
The grading for R 415 as a function of the VCO slope is as follows for factory alignment:

S_{VCO} = 500 kHz/v to 560 kHz/V	3k32
S_{VCO} = 560 kHz/v to 620 kHz/V	2k94
S_{VCO} = 620 kHz/v to 680 kHz/V	2k74
S_{VCO} = 680 kHz/v to 740 kHz/V	2k49

Note: The VCO slope itself need not be checked as long as one of the above R 415 values complies with the tolerances for the control limit frequencies.

7.2.4.3 Sawtooth phase meter alignment

7.2.4.3.1 Switching threshold (7 P 301)

Test setup:
- Connect the DVM at 7 TP 1 (+) and 7 TP 2 (-).
  Important: Make sure the polarity is correct!
- Do not apply an input signal!

Alignment:
- Use 7 P 301 to align: +100 mV $\pm$ 10 mV

7.2.4.3.2 Symmetry (7 C 327)

Instruments:
- Generator, 1 MHz - 160 MHz, 0 dBm, e.g. PS-16 or SNA-1 and PSS-16
- DVM
- Oscilloscope: BW = 20 MHz

Settings:
- Set the EXTERNAL bit rate on the PJM-4
  (do not apply an external clock!)

Test setup:
- Feed the PJM-4 with the generator signal
- Connect the oscilloscope to output 7 TP 5 ($U_{\varphi 2}$).

Alignment:
- Vary the generator frequency at a high sweep rate (e.g. SNA-1 -> SWT 0.5 s).
- At the highest input sensitivity (AC) on the oscilloscope, use 7 C 327 to minimize the voltage fluctuation.

Check:

Test setup:
- Feed the PJM-4 with the generator signal
- Connect the DVM to output 7 TP 5 ($U_{\varphi 2}$)

Check:
- Slowly vary the generator frequency from 1 MHz to 160 MHz
- The voltage fluctuation as a function of generator frequency must be

$$|U_{\varphi 2\ max} - U_{\varphi 2\ min}| \leq 40\ mV.$$

Alignments affected:

7 P 302	Section 7.2.4.3.3
Code error	Section 7.2.3
Mixer	Section 7.2.4.4

7.2.4.3.3 Reference voltage (7 P 302)

Instruments:
- PJG-4
- Oscilloscope, BW = 20 MHz
- DVM

Settings:
- 139 Mbit/s, clock, switch off modulation on PJG-4

Alignment:
- 1. Coarse aligment:
  - Do not apply an input signal
  - Connect the DVM at 7 TP 4 (U_{REF2}) and 7 TP 5 ($U_{\varphi 2}$):
    Use 7 P 302 to align to 0 V

2. Fine alignment:
  - Apply an input signal
  - Connect the oscilloscope at 7 TP 5/AC
  - On the PJM-4, use the "ENTW" test menu (see Sections 9.3.1 and 9.3.2) to set a REGELGRENZFREQUENZ = 2 kHz; the PJM-4 must remain locked-in.
  - Use the DVM to check the voltage between 7 TP 4 and 7 TP 5:
    If U > 10 mV, Controller 2 is faulty and alignment is not possible.
  - On the PJG-4: Switch on Sinus Mod., 20 kHz
  - Slowly increase the jitter span (up to approx. 0.7 UI) and observe the modulation on the oscilloscope:
    Use 7 P 302 to align to symmetrical limitation
  - After alignment, use the test menu to set the REGELGRENZFREQUENZ to "AUTO".

Alignment affected: Mixer Section 7.2.4.4

7.2.4.4 Mixer alignment

7.2.4.4.1 90° phase (7 C 106)

Instruments:
- Oscilloscope, BW $\geq$ 100 MHz (e.g. TEK 2465)
- Bit rate generator, e.g. PF-4 or PJG-4
- Adapter card AK 3 (901-C)

Test setup:

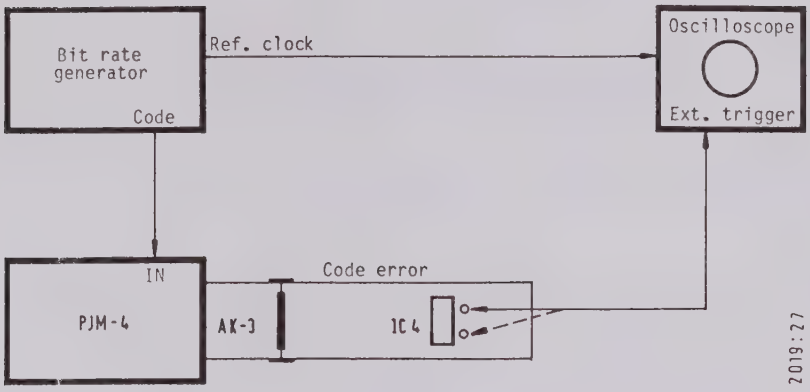


Fig. 7.2.4-1 90° phase alignment

Settings:

PJM-4	8448 kbit/s, AMI, LEADING EDGE, put code error card onto AK 3
PJG-4	8448 kbit/s, AMI, continuous 1"
Oscilloscope	External triggering from bit rate generator

Check:
- With test probe on code error card at 3 IC 4, Pin 6 (ground, Pin 9): Expand the pulse so that it covers 8 divisions symmetrically about the middle of the screen.
- With the same test probe at 3 IC 4, Pin 5 (ground, Pin 9): The clock edge now visible must be in the middle of the screen (90° lag):

  Tolerance: $\pm$ 4.5° $\cong$ $\pm$ 0.2 divisions

Alignment:
- Use 7 C 106 to align, if necessary.

7.2.4.4.2 440 MHz wave trap (7 C 111)

Instruments: SNA-1 analyzer with TK-11 active test probe

Settings: PJM-4 139 Mbit/s,
Open Dip-Fix switch 7 S 401 in Controller 2 and connect control voltage output 7 Pt. 46 to ground

Analyzer F_{span} = 20 MHz/Div
F_{cent} = 80 MHz
RBW/VBW/INPUT ATT AUTO ON

Alignment: Connect the test probe in the 170 MHz LP 0° at 7 Pt. 16:
Use 7 C 111 to minimize the 80 MHz line.

7.2.5 11 MHz CIRCUIT (E)

7.2.5.1 11 MHz phase meter alignment (8 P 2)

Do not align!
In the event of a fault, board [2019-G] must be replaced by an aligned board.

Alignments affected: 10 P 101 Adder Section 7.2.6

7.2.5.2 20:1 divider (8 C 106)

Instruments: TEK 495A analyzer with TEK P6201 active test probe

Settings: PJM-4 No input signal, or locked-in at any bit rate

Alignment: With the active test probe at output 8 Pt. 3 of the 20:1 divider:
Use 8 C 106 to minimize the 220 MHz line.

7.2.5.3 11 MHz filter (8 L 201, 8 L 202)

Instruments: SPM-19 or SNA-1
with TK-11 active test probe

Settings: PJM-4 No input signal, or locked-in at any bit rate

Alignment: With the active test probe at output 8 Pt. 24 of the 11 MHz filter:
Use 8 L 201 to minimize the 22 MHz line.
Use 8 L 202 to minimize the 11 MHz line.

7.2.5.4 Controller 1 alignment

Pre-setting: - If the replacement board is not aligned, trimmer 9 P 2 must be pre-set in order to prevent oscillation of the 11 MHz circuit:

Turn trimmer 9 P 2 to the left-hand stop.

7.2.5.4.1 Gain (9 P 2) (2 Hz alignment)

Instruments: - PJG-4

Settings:
- PJM-4 34 Mbit/s, clock, HP = 2 Hz, LP = 600 kHz
- PJG-4: 34 Mbit/s, clock, Sinus Mod., 1 kHz, 1 UI

Alignment:
- Note the value displayed at 1 kHz and 1 UI = X
- Set 2 Hz, 1 UI:
  Use 9 P 2 to set the display to 0.7 x X.

7.2.5.4.2 11 MHz frequency (9 P 3)

Instruments: - Universal frequency counter for 11 MHz

Settings:
- Either apply no input signal or use the "ENTW" test menu to set REGLER 1 "KLEMM." (see Section 9.3)
- Fit the cover on the 11 MHz VCO

Alignment:
- Measure the frequency of the VCO at 8 Pt. 13 in the 11 MHz phase meter
  Use 9 P 3 to set 11 MHz $\pm$ 10 Hz.

Check:
- With the same instrument settings (!) use the DVM to measure the voltage at 9 Pt. 4 in Controller 1:
  Required: $-2\ V \leq U \leq 2\ V$

7.2.5.4.3 Lock-in aid (9 P 1)

Instruments:
- PJG-4
- TR 940 or digital storage oscilloscope
- Oscilloscope, BW = 20 MHz

Settings:
- PJM-4 139 Mbit/s, Data, CMI
- PJG-4 139 Mbit/s, Data, CMI, random sequence $2^{10}-1$
  Sinus Mod., 20 Hz, 16 UI
- TR 940 DC Input, 500 mV/Div, 1:1 test probe
  TIME BASE 200 ms/Div, START mode (continuous recording)
- PJM-4 Connect DEMOD [9] to TR 940 input [11]

Alignment:
- Make the PJM-4 lock in/unlock by briefly switching over the bit rate frequency on the PJG-4.
- Observe the locking of the 11 MHz loop on the oscilloscope:
  If no locking or renewed unlocking occurs following "fast/slow" switching, reduce the jitter span on the PJG-4.
- Use 9 P 1 to optimize "fast/slow" switching:
  See Figs. 7.2.5-1 to 7.2.5-3.

If the jitter span was reduced, increase it again and repeat the alignment:
Minimum lockable jitter span after alignment:
$J \geq 15$ UI at 20 Hz

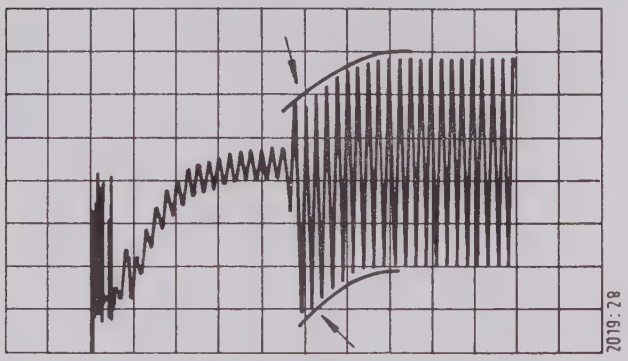


Fig. 7.2.5-1 Incorrect alignment of P 1

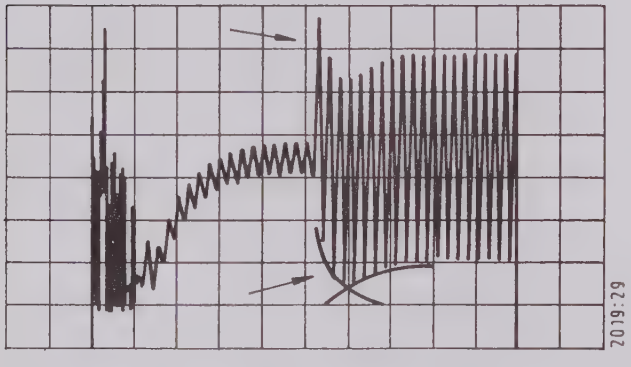


Fig. 7.2.5-2 Incorrect alignment of P 1

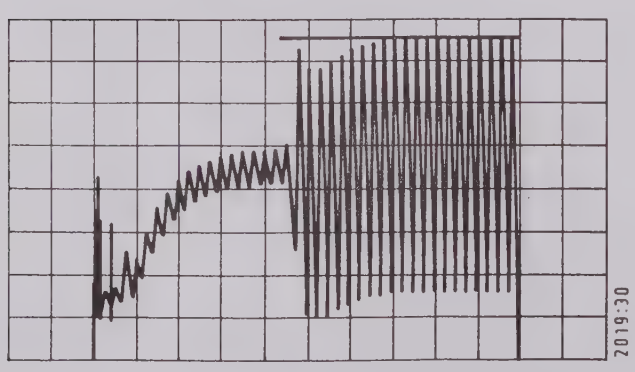
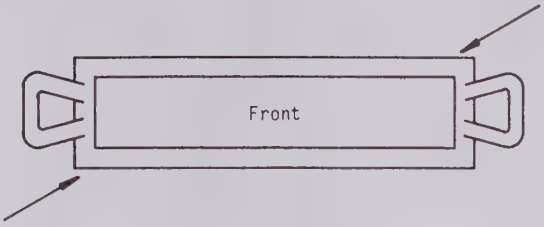


Fig. 7.2.5-3 Correct alignment of P 1

7.2.6 ADDER (F)

7.2.6.1 General information

Precondition:
- The entire instrument must warm up with all trough covers and the housing cover fitted loosely (see sketch):
  At least 1 hour at room temperature (22 °C)
  (internal temperature effect compensation of the phase meters)



Only undo 3 housing screws here

The upper housing section may then be removed for alignment.
The RF chassis can then also be swung up.

Important notes on alignment:
- The adder alignment should always be performed last when repairing the instrument.
- The order of alignment steps must be observed, since the various alignments mutually affect each other.

Pre-setting:
- If the replacement board is not aligned, Dip-Fix switches 10 S 1 ... 10 S 4 must be pre-set to any desired delay. See Fig. 7.2.6-1.

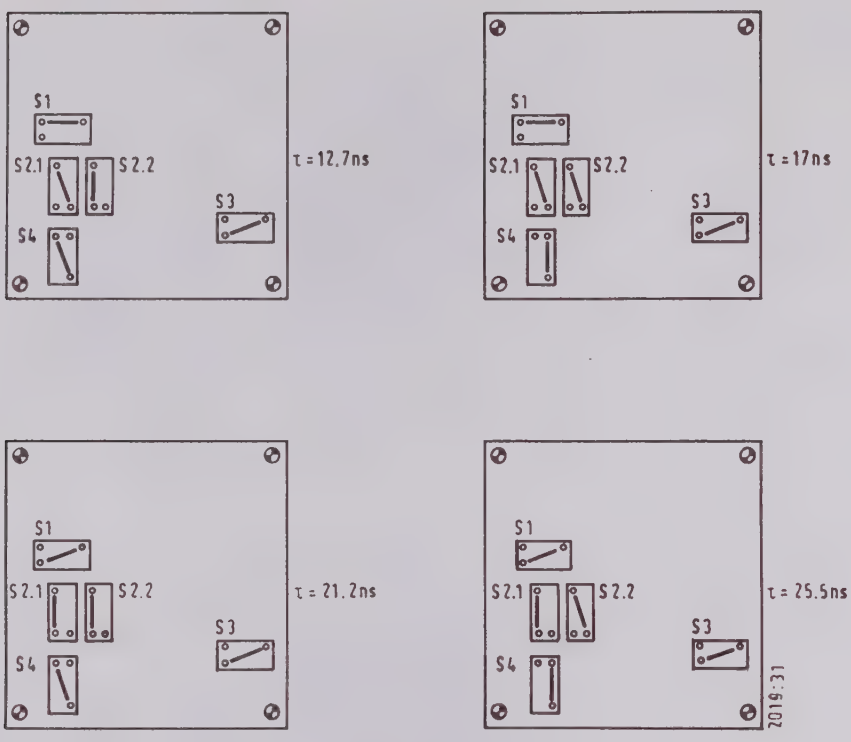


Fig. 7.2.6-1 Delay settings

Software aid: - "ENTW" test menu:
See Sections 9.3.1 and 9.3.2 for a description and how to call up.

Instruments: For alignment 7.2.6.3 (10 P 10, 10 P 11)
- DVM: 0.01 mV resolution

For all other alignments:
- PJG-4 Check the jitter frequency response at 1 UI on the oscilloscope!
- SNA-1 Version 02

Test setup:

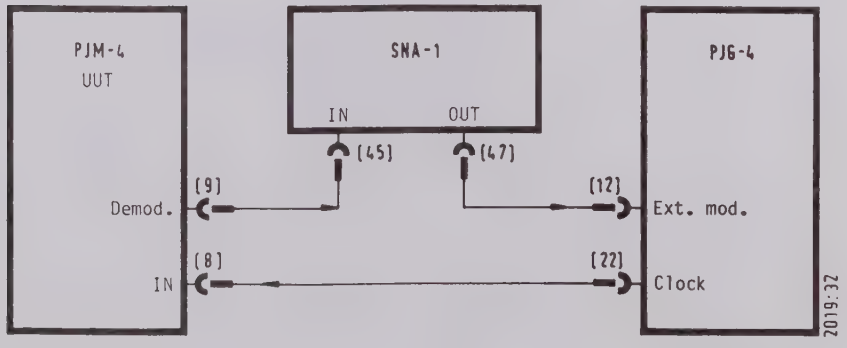


Fig. 7.2.6-2 Test setup for adder alignment

Settings: - PJG-4 Bit rate: 34 Mbit/s [1]
Code: NRZ/ECL
Clock: ECL [20]
Pattern: 1 ... 16, "10" sequence [15]
Ext. Mod.: 1.26 UI (corresponding to 0.445 UI, as SNA-1 send level only 0 dBm = -9 dB)

- PJM-4 Bit rate: 34 Mbit/s, CLOCK
Code: CMI
High-pass: 2 Hz
Low-pass: 6700 kHz

Note: It is normal for the illuminated fields "Bit rate" and "Low-pass" to flash at bit rates < 139 Mbit.

- SNA-1 NETWORK ANALYSIS
FSTART = 4 kHz, 3 DECADES
SCALE = 1 dB
ZERO-POS. = Middle of display
RBW = 300 Hz, VBW = 5 kHz, SWT = 2 sec
SEND LEVEL= 0 dBm
REFERENCE = -24 dB

Normalize the SNA-1:
Connect the SNA-1 input to the generator output,
-> "CAL/NORM" -> "Normalize MAG & PHS"

Check the setting:
-> REFERENCE = 0 dB -> The trace must be almost flat

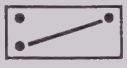
Restore the original test setup and reference setting.

7.2.6.2 11 MHz path gain (10 P 101)

Precondition: - See Section 7.2.6.1

Settings: - PJG-4 - 34.368 Mbit/s, CLOCK
- Int. Mod.: 1 UI, 20 kHz, Sine

- PJM-4 - 34.368 Mbit/s, CLOCK
- HP = 700 Hz, LP = 300 kHz
- Use the "ENTW" test menu to set the REGELGRENZFREQUENZ to 240 kHz
- Only switch on the 11 MHz path on the adder:
Close 10 S 3
Open 10 S 4



Alignment: - Press the "Mod. off" key on the PJG-4:
Note the jitter display = X
- Switch modulation on again on the PJG-4
- Use 10 P 101 to set:
Display = 1 UI + X ± 1 digit

Alignment affected:
- 220 MHz path gain Section 7.2.6.3

7.2.6.3 220 MHz path gain (10 P 102)

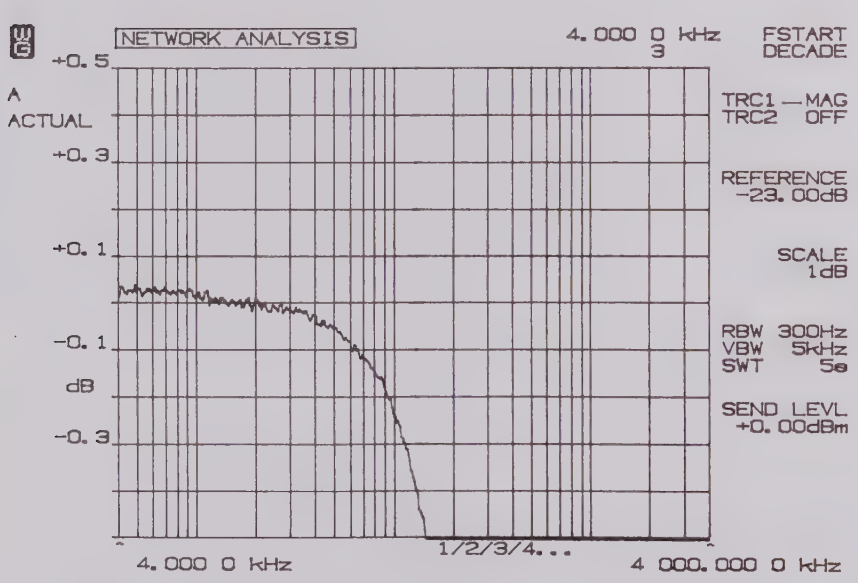
Preconditions:

Test setup: } See Section 7.2.6.1
Settings: } Bit rate: 34.368 Mbit/s, Clock

Alignment:

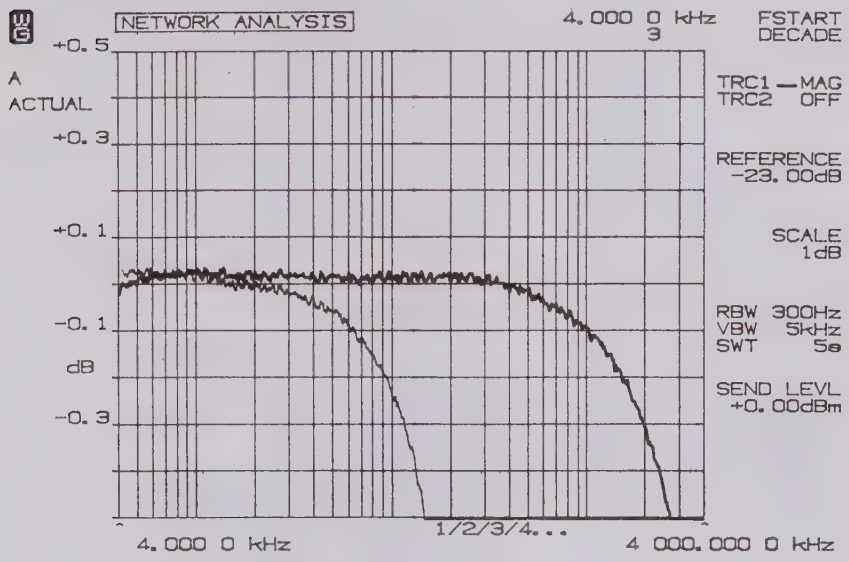
1. Determine the reference level of the aligned 11 MHz path:
   - Only switch on the 11 MHz path (see Section 7.2.6.2)
   - Use the "ENTW" test menu to set the REGELGRENZFREQUENZ = 240 kHz
   - Measure the signal level with the SNA-1 and set the straight section of the trace on the 0 dB line on the screen using REFERENCE.

   Store the trace as reference:



2. Alignment:
   - Switch on the 220 MHz path (10 S 4)
   - Set the REGELGRENZFREQUENZ = 2 kHz

     Use 10 P 102 to set the gain in such a way that the straight section of the measured level coincides with the reference curve:



7.2.6.4 Slope of the sawtooth phase meter for 2048 kbit/s

(14 P 1, current source DAC offset on RF control)

Preconditions: } See Section 7.2.6.1

Test setup: }

Note on procedure: The housing cover must be removed and the RF chassis swung up and open for the alignment.
In order to avoid errors due to thermal drift, all settings for the test setup should be made while the instrument is closed, so that the actual alignment can be carried out as quickly as possible.

Alignment:
- Switch on the 11 MHz path and 220 MHz path
- Use the "ENTW" test menu to set a REGELGRENZFREQUENZ = 2 kHz
- Set the bit rate 34.368 Mbit/s on the PJG-4 and PJM-4:

  Measure the Demod. signal with the SNA-1 and store the trace in <M> as reference.

- Set the bit rate 2.048 Mbit/s and measure with the same SNA-1 settings:

  Use 14 P 1 to align the trace (in the range up to approx. 20 kHz) to coincide with the reference curve in <M>.

After alignment: - Swing the RF chassis back in, replace the housing cover and allow the instrument to warm up again.

Check: - Repeat the measurement for all bit rate frequencies:

The deviations from the reference curve (34.368 Mbit/s) should not exceed the following values in the range up to approx. 20 kHz:

< 35 Mbit/s: ± 0.2 dB

> 35 Mbit/s: + 0.4 dB/-0.2 dB

See Fig. 7.2.6-3

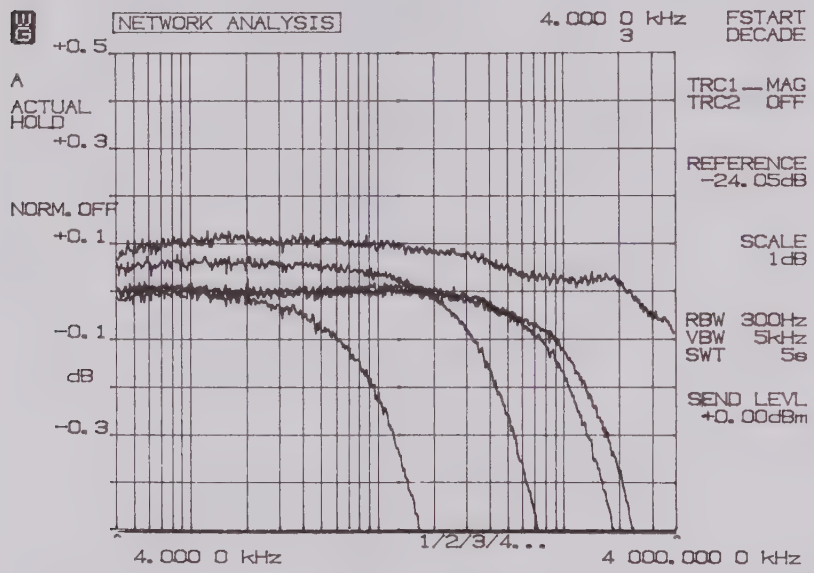


Fig. 7.2.6-3 Typical frequency responses, 220 MHz circuit; control limit frequency 2 kHz

7.2.6.5 Current source zero point (10 P 10, P 11)

Settings:
- PJG-4 Any
- PJM-4 Use the "PRUEFFELD" test menu to set the charging current for the sawtooth phase meter to 0.023 mA (corresponding to 704 kbit/s): -> "PRUEFFELD" -> "STROMQUELLE .023 mA"
- DVM Select the measuring range with 0.01 mV resolution

Alignment:
- Measure the voltage drop across 10 R 18/10 R 19:
  Required: 2.89 mV ± 0.1 mV
- Then set: across 10 R 18 with 10 P 11
  across 10 R 19 with 10 P 10
- After alignment, use the "TRAEGERPHASENMESSER" test menu to set "AUTO"

7.2.6.6 Frequency response compensation (10 C 128, C 108)

Preconditions: } See Section 7.2.6.1
Test setup: }

Settings:
- As in Section 7.2.6.1

Differences:
- Set the bit rate 139.264 Mbit/s on the PJG-4 and PJM-4
- Use the "ENTW" test menu to set the REGELGRENZFREQUENZ = 2 kHz

Alignment:
- Minimize the frequency response

in the range 1 - 3 MHz: with 10 C 128
in the range > 3 MHz : with 10 C 108

Note: Do not set any overshoot!
The frequency response must continue to show a downward trend towards high frequencies.

Check: Check the overall frequency response as per Section 7.2.6.8.

7.2.6.7 LP filter cutoff frequency (10 C 104)

Preconditions: } See Section 7.2.6.1
Test setup: }

Settings:
- As in Section 7.2.6.1

Differences:
- Bit rate: - 2.048 and 8.448 Mbit/s
- PJM-4 : - Use the "ENTW" test menu to set "AUTO" REGELGRENZFREQUENZ or "TEST AUS"

Alignment:
- Use 10 C 104 to set the max. frequency response rise:

8 Mbit/s: Set the max. rise in the range 300 - 500 kHz:
+0.15 dB +/- 0.05 dB
2 Mbit/s: Check the rise in the range 60 - 100 kHz:
+0.15 dB +/- 0.05 dB

- If necessary, correct the alignment until the tolerance limits are observed.

Tolerance limits:

2.048 Mbit/s 8.448 Mbit/s	f < 50 kHz f < 200 kHz	f < 100 kHz f < 400 kHz	f = 100 kHz f = 400 kHz
Limits	+0.05 dB -0.05 dB	+0.20 dB -0.05 dB	+0.20 dB -0 dB

7.2.6.8 Delay correction (10 S 1 ... S 4)

Preconditions:
Test setup:
} See Section 7.2.6.1

Settings:

- As in Section 7.2.6.1

Differences:

- Bit rate: - 139.264 Mbit/s, CLOCK
- PJM-4 : - Normal mode; to do so, use the "ENTW" test menu to select "TEST AUS" or switch the instrument off and back on

Alignment:

- By selecting one of the four possible delays with Dip-Fix switches 10 S 1 to 10 S 4 (Fig. 7.2.6-1), align to minimum frequency response in the range:
  100 kHz < f < 1 MHz
- Note:
  The gain in the 220 MHz path changes with each new delay setting. Therefore, repeat the alignment in Section 7.2.6.3 for each new setting.
- For further optimization, correct the frequency response with 10 C 128 and 10 C 108, if necessary.

Check:

When operated with a clock signal, the frequency response of the PJM-4 must be within the tolerances given below at all PJG-4 bit rates:
The reference value is the level at f = 4 kHz

Frequency range	Tolerance
4 kHz < f < 300 kHz	+/- 0.2 dB
300 kHz < f < 1 MHz	+/- 0.3 dB
1 MHz < f < 3 MHz	+/- 0.5 dB
3 MHz < f < 4 MHz	+/- 1.0 dB

Limitations of the frequency range:

2.048 Mbit/s	up to 100 kHz
8.448 Mbit/s	up to 400 kHz
25.776 Mbit/s	up to 800 kHz
34.368 Mbit/s	up to 800 kHz
139.264 Mbit/s	up to 4 MHz

Alignments affected:

- 220 MHz path gain	Section 7.2.6.3
- LP filter cutoff frequency	Section 7.2.6.7

7.2.7 FILTER (H)

If the cards Filter (11) and Peak rectifier (12) are replaced as a complete unit, no alignment work is necessary; the circuit boards are aligned at the factory.

7.2.7.1 Demodulator output slope (11 P 2)

Instruments:
- 1 Jitter generator PJG-4 W&G
- 1 Oscilloscope BW > 20 MHz
- 1 DVM 8050A, 8600A Fluke

Test setup: Connect clock output [22], PJG-4, with input [8], PJM-4.

Settings:
- PJG-4 8448 kbit/s, Clock, ECL
  Modulation: Sine
  Jitter : 10 UI, 1 kHz
- PJM-4 8448 kbit/s, Clock
  Code: NRZ/ECL
  High-pass: 2 Hz
  Low-pass : 300 kHz

Use the DVM to measure at 10 TP 1 (range 3 V AC).

$U_{TP\ 1} \approx 2.5$ V AC; note the value measured.

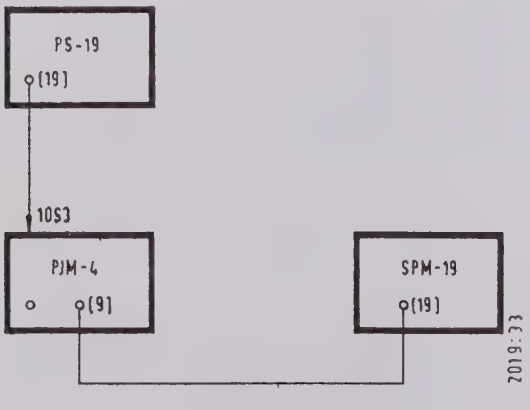
Terminate demodulator output [9] with 75 Ω and measure across the terminating resistor with the DVM.

Use (11) P 2 to set 0.1566 x $U_{TP\ 1}$.

7.2.7.2 Demodulator output frequency response (11 C 37)

Instruments: - Level measuring setup PS(S)-19/SPM-19

Test setup:



UUT A: Set (10) S 3 to R 101 and feed onto bow of (10) S 3 with coaxial cable.

Settings:
- PS-19: 1 kHz, -10 dBm; Z = 75 Ω
- SPM-19: MODE DGTL; f = 1 kHz; Z = 75 Ω
- UUT: High-pass: 2 Hz; Low-pass : 6700 kHz

Store the measured value on the SPM-19 (ABS -> REF).
Switch on differential measurement (ABS - REF).
Set the PS-19 and the SPM-19 to f = 3.86 MHz.

Use (11) C 37 to set the display on the SPM-19 to +0.1 dB.

7.2.8 PEAK RECTIFIER (K)

7.2.8.1 30 dB amplifier gain (12 P 1)

Instruments:
- 1 Jitter generator PJG-4 W&G
- 1 DVM 8050 A, 8600 A Fluke
- 1 Level generator PS-19 W&G

Test setup: Connect clock output [22], PJG-4, to input [8], PJM-4.
Connect the PS-19 to 10 S 3; see test setup 7.2.7.2 (the SPM-19 is not needed).

Settings:
- PJG-4: 8448 kbit/s, Clock, ECL; Modulation: OFF
- PJM-4: 8448 kbit/s, Clock, NRC ECL; High-pass: 2 Hz; Low-pass : 6700 kHz

Alignment: PS-19 f = 1 kHz; Level: -10 dBm
Use the RMS-DVM to measure at (12) Rel 1 Pt. 3 and (12) R 5. Note the result.

PS-19 Level: -40 dBm
Use (12) P 1 to align the value at (12) Rel 1 Pt. 3 to the previously measured value.

7.2.8.2 Offset alignment (12 P 4, 12 P 5)

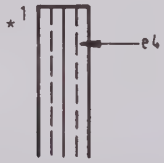
Test setup:

Settings: PJG-4 Bit rate: 8448 kbit/s
Jitter modulation OFF
Clock ECL

PJM-4 Bit rate: 8448 kbit/s CMI
Low-pass : 74 kHz
High-pass: 900 kHz

Connect anode (12) Gl 1 and cathode Gl 3 to ground (shortest possible connection).
If the jitter display reads 1 mUI, no offset alignment is necessary.

Alignment: Use the oscilloscope to measure at (12) Pt. e 4* and align the signal to 0 V with P 4 and P 5.
Do not apply an input signal during the alignment.



7.2.8.3 Peak value meter gain (12 P 2, P 3)

Test setup: As in Section 7.2.8.2

Settings: - PJG-4 Bit rate : 8448 kbit/s
Jitter modulation: Sine, 1 kHz, 1 UI
Clock ECL

- PJM-4 Bit rate : 8448 kbit/s
Low-pass : 600 kHz
High-pass: 100 Hz

Measure the signal with an RMS voltmeter/AC (e.g. Fluke 8050A, 8600A) at (11) Pt. 12 c. Note the result.

+Û alignment

Switch the PJM-4 jitter display to +p.
Use (12) P 3 to set the jitter display to 2.02 x measured value.

-Û alignment

Switch the PJM-4 jitter display to -p.
Use (12) P 2 to set the jitter display to 2.02 x measured value.

7.2.8.4 Frequency response alignment (12 C 405, C 205)

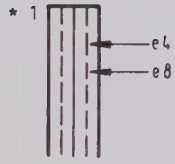
Instruments:
- 1 Jitter generator PJG-4 W&G
- 1 DVM 8050A, 8600A Fluke
- 1 Level generator PS-19 W&G

Test setup: Connect clock output [22], PJG-4, to input [8], PJM-4.
Connect the PS-19 to 10 S 3; see test setup 7.2.7.2 (the SPM-19 is not needed).

Settings:
- PJG-4 34 Mbit/s
  Modulation: OFF
- PJM-4 34 Mbit/s, Clock, NRC ECL
  High-pass: 2 Hz
  Low-pass : 6700 kHz

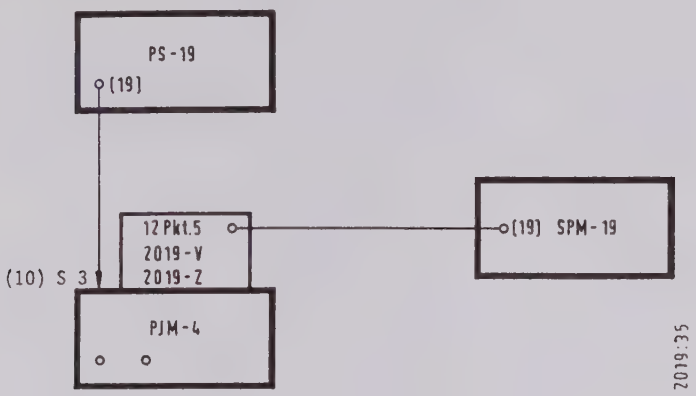
Alignment: Connect clock conversion at (12) e 8* to ground.
Connect the digital multimeter at (12) Pt. e 4*.
Measuring range VDC

- PS-19 f = 1 kHz
  L = -10 dBm
  Note the measured value (approx. 1.25 V)
- PS-19 f = 3.86 MHz
  Use (12) C 405 [2019-AG] to set the DVM display to the previously measured value x 1.006.
- PS-19 f = 1 kHz
  L = -40 dBm
  Note the measured value.
- PS-19 f = 3.86 MHz
  Use (12) C 205 [2019-AH] to set the DVM display to the previously measured value.



7.2.8.5 Hit counter frequency response (12 C 305)

Test setup:



UUT	Set (10) S 3 to R 101 and feed to bow of (10) S 3 with coaxial cable.
SPM-19	Connect the coaxial cable to (12) Pt. 5.
PS-19	f = 1 kHz, -10 dBm Z = 75 Ω
SPM-19	f = 1 kHz MODE DGTL Z = 75 Ω
UUT	High-pass: 2 Hz Low-pass : 6700 kHz

Store the measured value on the SPM-19 (ABS -> REF).
Switch on differential measurement (ABS - REF).
Set the PS-19 and the SPM-19 to f = 3.86 MHz.
Use (12) C 305 to set the display on the SPM-19 to +0.1 dB.

7.2.9 HIT COUNTER (I)

7.2.9.1 Gain (13 P 1) and offset (13 P 2, 13 P 3)

Instruments: - PJG-4

Settings:

- PJG-4
  - Bit rate : 25.776 Mbit/s, CLOCK
  - Code : NRZ/ECL
  - Int. Mod. : 1 kHz, Sine
- PJM-4
  - Bit rate : 25.776 Mbit/s
  - Code : NRZ/ECL
  - HP = 100 Hz, LP = 74 kHz
  - Phase hits : ON
  - Count. status: START MAN., GATING REP., 1 s (See Section 3.3.4.1 of Operating Instructions)
  - Counter mode : RESULT DISP. ABSOL. (See Section 3.3.5.1 of Operating Instructions)

Alignment:

1. Align positive counter threshold:
   Set (+) PEAK jitter measurement on the PJM-4

1.1 Set THRESHOLD to 7.99 UI
Start counting with the START/STOP key and increase the jitter span on the PJG-4 until the PJM-4 display = 8 UI (note the exact value = X)

Use 13 P 3 to align the counting result to:
Counter reading = 500 ± 200

1.2 Set THRESHOLD to 7 UI, start counting and reduce the jitter span on the PJG-4 until counter reading = 500 ± 200

If the jitter span displayed on the PJM-4 is greater/less than X-1, turn 13 P 1 clockwise/anti-clockwise (about 2 turns to start)

1.3 Repeat from 1.1 until the jitter span displayed on the PJM-4 is:
[(X-1) ± 0.05] UI

1.4 Set THRESHOLD to 0.1 UI, start counting and set the jitter span on the PJG-4 in such a way that the PJM-4 displays 0.1 UI.

Use 13 P 3 to set the counter to 500 ± 200 (max. 0.5 turns; if more, align again with higher jitter).

1.5 The following must apply:
Display = 0.12 UI => Counter reading > 0.98 x f_{mod}
Display = 0.08 UI => Counter reading < 0.02 x f_{mod}
(f_{mod} measured with counter at Demod. output)

2. Align the negative counter threshold:

2.1 Set (-) PEAK jitter measurement on the PJM-4 and set the jitter span on the PJG-4 in such a way that the PJM-4 displays 0.1 UI.

Use 13 P 2 to align the counting result to:
500 ± 200

2.2 As under 1.5

2.3 At a THRESHOLD setting of 7 UI or 8 UI, a counter reading of 500 ± 200 should be reached with a jitter display of:
7 or 8 UI ± 0.1 UI

3. Check the PEAK-PEAK threshold:

With

Jitter display	0.2	2	6	14	UI_{pp}
THRESHOLD	0.1	1	3	7	UI_{p}

the counter display should read:
1000 ± 400

In the event of deviations, check the alignments again.

7.2.9.2 Real-time clock (13 C 6)

Instruments: - Universal frequency counter with 10:1 test probe

Settings: - PJM-4 Operate without the filter/rectifier card (accessibility of 13 C 6)
- Counter Period measurement

Alignment: - Connect the test probe to 13 TP 15 and use 13 C 6 to set the period:
T = (1,000,000.0 ± 0.5) µs

7.2.10 RF CONTROL

7.2.10.1 Charging current I_{ps} (14 P 2)

Test setup: - Connect the DVM in the sawtooth phase meter (!) [7/2019-0] across 7 R 341.

Settings: - On the PJM-4, use the "PRUEFFELD" test menu to set 4.6 mA STROMQUELLE.

Alignment: - Use 14 P 2 to align to 4.6 V ± 0.01 V.

Alignment affected:
- 220 MHz path gain Section 7.2.6.3

7.2.10.2 Current source DAC offset (14 P 1)

Align in accordance with Section 7.2.6.4.

7.2.10.3 -5.2 V setting (14 P 3)

Test setup: - Connect the DVM in the 11 MHz phase meter [8/2019-G] at 8 Pt. 12.

Alignment: - Use 14 P 3 to set:
-5.2 V ± 0.02 V

7.2.10.4 Equalizer amplifier alignment (14 P 5, P 6, P 7)

Instruments: - PJG-4
- TR 940 or digital storage oscilloscope
- Oscilloscope: BW > 20 MHz

Settings: - PJG-4 139 Mbit/s, Clock, modulation: OFF
- PJM-4 139 Mbit/s, Clock, HP = 2 Hz, LP = 600 kHz
- TR 940 Input A, DC, 0.05 V/Div., Playback A & B, Start mode

Alignment:
- Turn 14 P 7 to the left-hand stop
- Connect the DVM at Demod. output [30]:
  Use 14 P 5 to align to 0 V
- Switch on modulation on the PJG-4:
  200 Hz, Sine, 1 UI
- Connect the TR 940 at Demod. output [9] and store the measured signal as reference (A --> B)
- Connect the TR 940 at Demod. output [30]:
  Use 14 P 6 to make the trace coincide with the reference curve.

Note: If no TR 940 is available, the alignment (14 P 6) can be carried out with a 2-channel oscilloscope. In this case, the measured result includes the inaccuracy of the oscilloscope.

7.2.11 POWER SUPPLY UNIT (N)

7.2.11.1 Complete power supply unit

If the complete power supply unit is replaced, no alignment is necessary.

7.2.11.2 DC/DC modules

No alignment is necessary after replacing individual DC/DC modules.

7.2.11.3 -5.2 V linear controller

The +12 V, -12 V, +5 V converters may be removed.

Series A: Small board on the rear of the wiring card.
Series B: The linear controller is on the charging circuit board.
The check and the alignment can be performed in the power supply unit.
With 220 V mains voltage, Pt. 34 -> 36⊥ should have -6,3 V-.

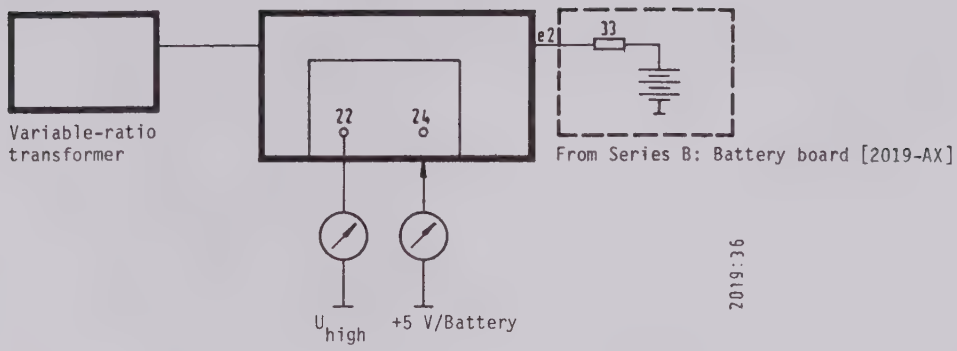
Check the voltages at the power transistor:
E: -6.3 V
C: -5.25 V
Pt. 37 -> 36⊥ : Set -5.25 V with P 5

7.2.11.4 Charging circuit

The +12 V, -12 V, -6.3 V converters may be removed.

The measurement and the alignment can be performed in the instrument.

Test setup:



Measurement and alignment of the switching threshold:

220 V variable-ratio transformer, high-end voltage check: Pt. 22: +30 V-
+5 V check Pt. 23: +5.0 V ± 0.1 V

Use a 100 kΩ/V instrument to measure the voltage at Pt. 24: +5.0 V

Turn down the mains voltage on the variable-ratio transformer and observe the high-end voltage at Pt. 22 and the DR voltage at Pt. 24.

When U_{ob} = 17.5 V ± 0.2 V is reached, T 2 switches from +5 V voltage to 3.5 ... 4 V battery voltage.

Turn up the mains voltage. When the high-end voltage is 19 V ± 0.2 V, T 2 should switch back from the battery voltage to +5 V.

The lower switching threshold can be set on P 1, the upper swiching threshold on P 2.

Anti-clockwise: Lower threshold voltage.

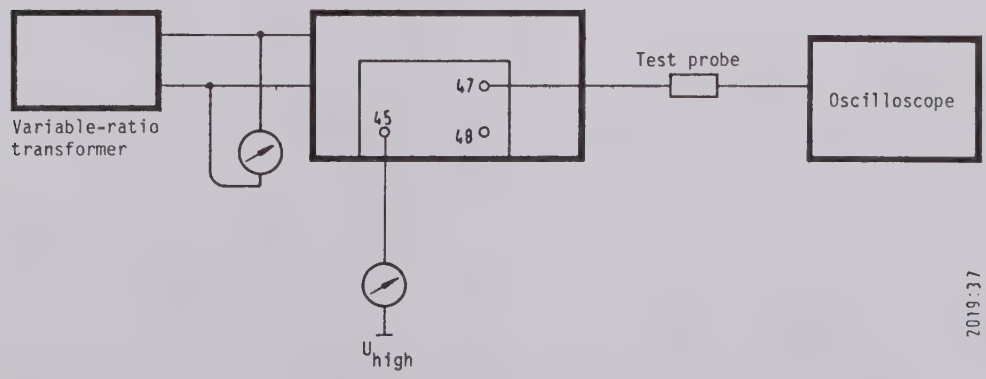
Caution: Setting one switching threshold also affects the other. Therefore, always check both thresholds.

7.2.11.5 Control unit

No DC/DC converters are required.

The measurement and the alignment can be performed in the power supply unit.

Test setup:



With 220 V mains, check the high-end voltage at Pt. 45: +30 V

Sync. voltage

Mains voltage 220 V
Connect the oscilloscope with test probe at Pt. 47.
Oscilloscope: AC 0.1 V/cm 0.5 µs/cm

Measure the pulse voltage:

Pulse height : 5 ... 6 V_{pp}
Pulse width : 300 ns ± 100 ns
Pulse interval: 24.7 µs ± 0.2 µs

The pulse interval can also be measured with a counter with 1 MHz LP: 405 kHz.
The frequency can be set with P 10.
Also check the sync. voltage at the inputs of the DC/DC converters.
Pt. a C, b C, d C, c C.

7.2.11.6 Data-save signal

Test setup as above, but without oscilloscope.
Slowly increase the mains voltage, observing the data-save signal at Pt. 48; measure the high-end voltage.
The DR voltage rises to 2.5 ... 5 V; when a mains voltage of approx. 140 V is reached, it suddenly drops to < 0.8 V.
Required high-end voltage: 19 V ± 0.2 V
Turn down the mains voltage until the DR signal re-appears. Required high-end voltage: 16.5 V ± 0.5 V
The switching threshold > 2.5 V -> < 0.8 V can be set with P 11.
(Potentiometer anti-clockwise -> Higher threshold)

Also check the signal at Pt. e 15.

8 VERIFICATION OF TECHNICAL DATA 8-1

8.1 Introduction 8-1

8.2 Function tests 8-2
8.2.1 Jitter measurements 8-2
8.2.1.1 Clock and data signals 8-2
8.2.1.2 Weighting filter 8-3
8.2.2 Phase threshold transgressions 8-3
8.2.2.1 Threshold errors 8-4
8.2.3 Code error detection 8-5

8.3 Return losses 8-6
8.3.1 Return losses in the range 10 kHz ... 15 MHz 8-6
8.3.2 Return loss measurements in the range 15 MHz ... 180 MHz 8-7

8.4 Input sensitivity, equalization 8-8
8.4.1 Input sensitivity 8-9
8.4.1.1 Input sensitivity with binary signals 8-9
8.4.1.2 Input sensitivity with ternary signals 8-10
8.4.2 $\sqrt{F}$-law equalization 8-10

8.5 Synchronization, counting mode 8-12
8.5.1 Synchronization 8-12
8.5.2 Counting mode 8-13

8.6 Jitter measuring accuracy 8-14
8.6.1 Basic noise 8-15
8.6.2 Jitter display 8-16
8.6.2.1 Absolute display at various bit rates 8-17
8.6.2.2 Display linearity 8-17
8.6.2.3 Display frequency response 8-19

8 VERIFICATION OF TECHNICAL DATA

8.1 INTRODUCTION

This section describes techniques for checking all the important technical data and functions of the instrument.

This excludes data and functions which can be checked by the user without requiring any specific explanations, or which are automatically checked by a built-in test routine. As far as possible, commercially available test equipment is used. It is assumed that the instrument to be tested is fully operational.

Unless otherwise stated, the tests and any necessary adjustments should be carried out within the nominal range of use of ambient temperature and after the specified warm-up period has elapsed.

The technical data checks will establish whether the display or output of a measured quantity lies within the specified error limits of the instrument. The test results are absolute only if the uncertainty in the test equipment used is negligible. Wherever the use of commercially available equipment is likely to lead to a distortion of the results, a further method will be indicated which makes use of test equipment produced in the Wandel & Goltermann factory for this purpose. Such tests can only be performed at Wandel & Goltermann service points specifically equippec for this purpose and are headed "W&G factory tests".

The error of the test equipment used is always assigned to the item under test (see IEC Publication 359) when deciding whether or not the error limits have been exceeded.

In the case where errors are symmetrical about the mean value, the following principle holds true: if the error limit of the item under test is given as $\pm$ e, then

if the limit $\pm$ (e + m) is exceeded, then the specified error limits have definitely been exceeded, and

if the limit $\pm$ (e - m) is not exceeded, then the specified error limits have definitely not been exceeded.

As far as possible, the values of e and m are quoted for each test. Since the value of m is dependent on the test equipment used, it must be determined if equipment other than that specified in the test is used.

To ensure a systematic check of the technical data, we recommend that the test be carried out in the order in which they are given.

Adjustment of the item under test need only be carried out when the total determined error is greater than $\pm$ (e + m).

8.2 FUNCTION TESTS

Test equipment required:

1 Jitter Generator	PJG-4	from W&G
1 Bit Error Test Set	PF-4	from W&G

8.2.1 JITTER MEASUREMENTS

Figure 8.2-1 Test setup for jitter measurements

8.2.1.1 Clock and data signals

Instrument settings:

PJG-4:	Range	[5]: 0.00 to 2.40 UI_{pp}
	Jitter amplitude	[6] [7]: 0.40 UI_{pp}
	Filter frequency	[8] [9] [10] [11]: 1.0 kHz
	Modulation	[13]: Sinus
	Clock	[4]: Internal
PJM-4:	Filter	: LP and CCITT
	EDGE	[4]: TRAIL
	EQU	[4]: FLAT
	Result	: filter pp

Set the generator and the receiver using the following table. Read off and evaluate the jitter display (after synchronization). (Expected value approx. 0.35 to 0.45 UI_{pp}.)

PJG-4	together	PJM-4
Clock [22]	NRZ/TTL; 2048 8448 kbit/s 34368	Clock [4]
Signal [21]		
1010	NRZ/ECL; 2048 / 139264 kbit/s	
0000	CMI; 139264 kbit/s	
1111	CMI; 139264 kbit/s	
$10...0_{16}$	AMI; 2048 / 34368 kbit/s	Data [4]
$10...0_{16}$	NRZ/ECL; 139264 kbit/s	
$2^{23}-1$	NRZ/ECL; 2048 139264 kbit/s	

Figure 8.2-2 Table for input signal settings

8.2.1.2 Weighting filter

Instrument settings:

PJG-4:	Range	[5]: 0.00 to 2.40 UI_{pp}
	Jitter amplitude	[6] [7]: 0.40 UI_{pp}
	Modulation	[13]: Sinus
	Clock	[4]: Internal
	Code	[20] [19]: NRZ/ECL
	Bit rate	[1]: 139264 kbit/s
	Pattern	[15]: 10
PJM-4:	Input	[4]: DATA
	Filter	: MAN, HP 2 Hz, LP 6700 kHz
	Polarity	[4]: TRAIL
	EQU	[4]: FLAT
	Result	: filter pp
	Code	: NRZ/ECL
	Bit rate	: 139264 kbit/s

With applied signal and 1 kHz filter frequency ([8] to [11] PJG-4), read off and note down the reference value on the device under test (DUT). Then set the filter cutoff frequencies (using the following table) on the PJM-4 and select the corresponding filter frequency on the PJG-4. Read off the new display on the PJM-4. Expected display reduction of 30 % (-3 dB) compared to the reference value.

Highpass (HP) cutoff frequencies:

10, 20, 60, 100, 200, 700 Hz, 3, 8, 10, 18, 24, 32, 80, 160, 900 kHz

(LP remains at 6700 kHz)

Lowpass (LP) cutoff frequencies:

74, 185, 300, 600, 1200 kHz

(HP remains at 10 kHz)

8.2.2 PHASE THRESHOLD TRANSGRESSIONS

Figure 8.2-3 Test setup for phase hit measurements

8.2.2.1 Threshold errors

Instrument settings:

PJG-4:	Bit rate	[1]: 139264 kbit/s
	Clock	[4]: Internal
	Jitter frequency	[8] to [11]: 1 kHz
	Code	[20] [19]: NRZ/ECL
	Modulation	[13]: Sinus
PJM-4:	Input	[4]: CLOCK
	Filter	: MAN, HP 100 Hz
	Result	: filter & phase hits
	Gate time	: 1 s
	Bit rate	: 139264 kbit/s
	Code	: NRZ/ECL
	Polarity	[4]: TRAIL
	EQU	[4]: FLAT
	Gating	: REP

Set threshold value on the PJM-4 (via COUNT STATUS -> THRS) and start the counting mode ([5]). Adjust the jitter amplitude on the PJG-4 so that the counter result displays approx. 5.10^2 (i.e., the jitter test values exceed by half the threshold value set). Compare the jitter display of the PJM-4 with the threshold value set and determine any deviation. Carry out the measurements using the following table.

Settings on PJM-4 JITTER result	THRS	Specified error limit (e)	Test setup error (m)
+p -p	0.250 UI_p	$\pm$ 0.027 UI_p	$\pm$ 0.006
+p -p	1.000 UI_p	$\pm$ 0.080 UI_p	
+p -p	4.000UI_p	$\pm$ 0.290 UI_p	$\pm$ 0.006
+p -p	7.50 UI_p	$\pm$ 0.535 UI_p	

Figure 8.2-4 Table for phase hit measurements

8.2.3 CODE ERROR DETECTION

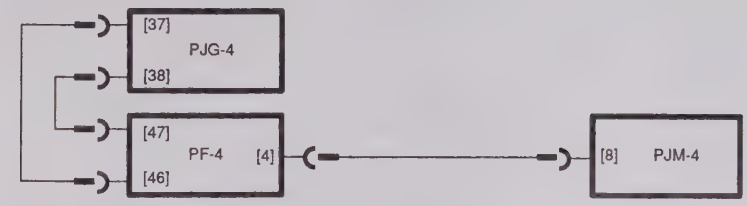


Figure 8.2-5 Test setup for detecting code errors

Instrument settings:

PJG-4:	Clock	[4]: PF-4
	Pattern	[15]: $2^{23}-1$
PF-4:	Clock	[6]: CAL
	Pattern	[10]: PSR $2^{23}-1$
	Error	[20]: Code
PJM-4:	Input	[4]: TRAIL; DATA; FLAT
	Filter	: MAN. HP 100 Hz LP 6700 Hz
	Average	: ON
	Result	: JITTER & CODE ERRORS INTERNAL
	Result display	: absolute
	Gating	: REP.
	Gating time	: 1 s

Code error detection should be checked for both unjittered and jittered signals, using the following table. For jittered signals, the jitter amplitude should be set so that the jitter display listed (approx.) appears on the PJM-4. Re-start the counting mode each time after changing any settings on the PJM-4 by pressing key [6].

Instrument settings						Results on PJM-4	
PJG-4 PJM-4 PF-4 Code	PJM-4 PF-4 Bit rate	PJG-4 Jitter frequency & amplitude	Modulation	PF-4 Error test [14]	Pattern [10], [11]	Code error	AIS
CMI	139264 kbit/s	5000 kHz & 0.27 UI_{pp}	OFF	ON, 10^{-3}	PRS-23	139264 ± 5	OFF
			Sinus	OFF	PRS-23	0	OFF
					DW 1		ON
AMI	34368 kbit/s	3000 kHz & 0.3 UI_{pp}	OFF	ON, 10^{-3}	PRS-23	34368 ± 1	OFF
			Sinus	OFF	DW 1	0	ON
		3000 kHz & 0.35 UI_{pp}			PRS-23		OFF

Figure 8.2-6 Table for code error detection

8.3 RETURN LOSSES

Instruments required:

1 Spectrum and network analyzer	SNA-1 from W & G
1 Return loss measuring attachment	RFZ-5 from W & G
1 Reflection coefficient measuring bridge	RFZ-4 from W & G

8.3.1 RETURN LOSSES IN THE RANGE 10 kHz ... 15 MHz

Instrument settings:

SNA 1:

MODE	[30]: Network analysis
CAL/NORM	[31]: CLR NORM
REFERENCE	: -65 dB
SCALE	: -50 dB
RBW	: 1 kHz
SWT	: 2 s
SEND LEVL	: 0 dBm

UUT:

CODE	: NRZ TTL

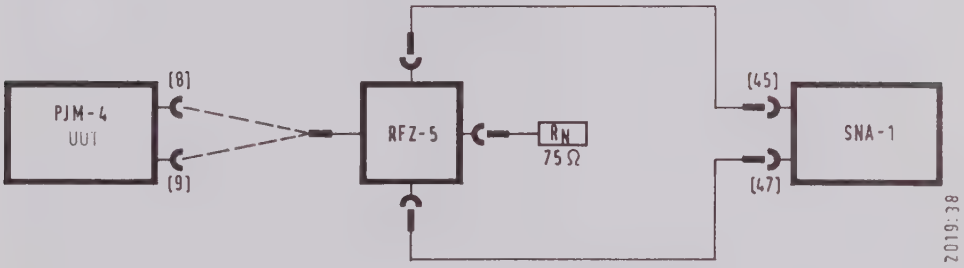


Fig. 8.3-1 Test setup for return loss measurements in the range 10 kHz ... 15 MHz

Test setup calibration:

Calibrate the return loss measuring attachment for sweep mode in accordance with the Operating Instructions.

Fit the standard resistor r = 0.1 on the measuring bridge in place of the UUT. Once the trace for a_r = 20 dB has been displayed on the screen, store the display (press "A" and "M" simultaneously), then press "A - M" [3]. The REFERENCE 0dB line now corresponds to a return loss of 20 dB.

Measure:

Connect the UUT to the measuring connection of the bridge. Make the settings given in the Table below and read the result on the screen (a_r = 20 dB - displayed level value).

UUT connection	SNA-1 FSTART	SNA-1 FSTOP	Specified error limit $a_r \geq$ (e)	Test setup error (m)
Input [8]	25 kHz	15 MHz	20 dB	± 0.54 dB
Demod. [9]	10 kHz	5 MHz	30 dB	± 0.72 dB

Fig. 8.3-2 Table for return loss measurements in the range 10 kHz ... 15 MHz

8.3.2 RETURN LOSS MEASUREMENTS IN THE RANGE 15 MHz ... 180 MHz

Instrument settings:

SNA-1:

MODE	[30]	: Network analysis
REFERENCE		: - 10 dB
FSTART		: 15 MHz
FSTOP		: 180 MHz
RBW		: 3 kHz
SWT		: 2 s
SEND LEVL		: 0 dBm
SCALE		: 50 dB

UUT:

CODE	: NRZ TTL

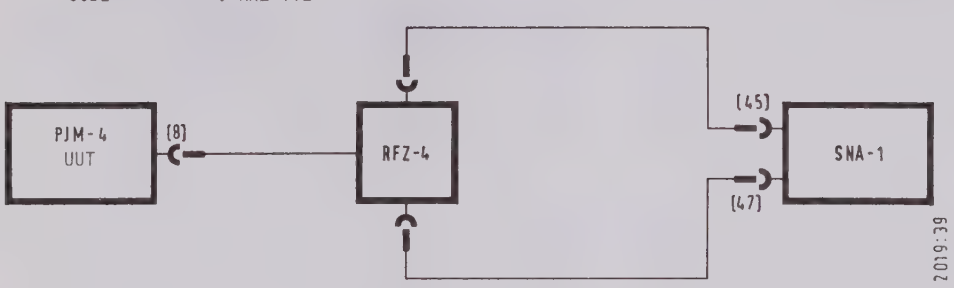


Fig. 8.3-3 Test setup for return loss measurements in the range 15 MHz ... 180 MHz

Test setup calibration:

Leave the measuring input of the bridge open and display the trace for a_r = 0 dB on the screen. Then store the display (press "A" and "M" simultaneously) and set "A - M" [3]. The REFERENCE 0 dB line now corresponds to a return loss of 0 dB.

Measure:

Connect the UUT to the measuring input of the bridge. Measure with the UUT divider settings 0, 10, 20 and 30 dB. These are called up via the test menus as follows: Press [STO & RCL] simultaneously, then page on through [ENTW] - [EING-STUFE] - [EING-TEILER] and select the required divider stage. (This status is indicated during the measurement by the word "TEST" instead of CONT STATUS).

At the end of the measurements, switch of the test menu as follows: [STO & RCL] - [ENTW] - [TEST AUS]

Specified error limit (e): a_r > 20 dB

Test setup error (m) : $\pm$ 0.63 dB

Note: The return loss can only be measured up to 180 MHz with the test setup given here. If verification up to 210 MHz is required, a different test setup must be used, such as the one shown below:

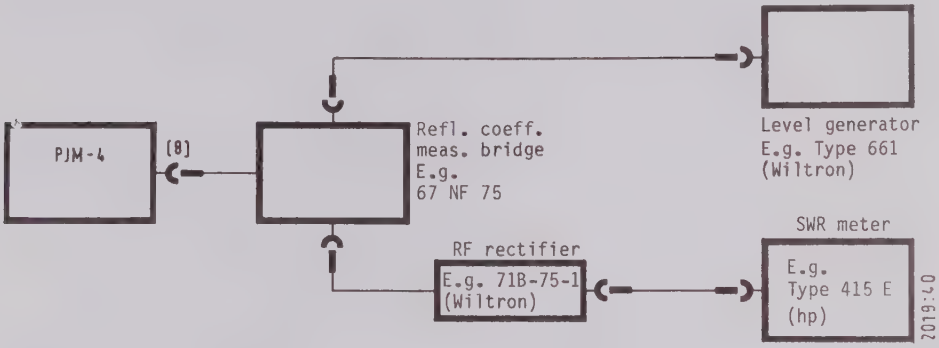


Fig. 8.3-4 Test setup for return loss measurements up to 210 MHz

8.4 INPUT SENSITIVITY, EQUALIZATION

Instruments required:

1 Oscilloscope	Type 2465	Tektronix
1 Jitter generator	PJG-4	W & G
1 Attenuator set (Z = 75 Ω)	D-2053	Siemens
1 Spectrum analyzer	SNA-1	W & G

Instrument settings:

PJG-4:

Clock	[4] : INTERNAL
Modulation	[13] : OFF
PATTERN	[15] : 1 ... 16
Digital word [16], [17],	[18] : 010101 ...
Bit rate	[1] : 139 264 kbit/s
Code	[19] : CMI

PJM-4:

Filter (HP/LP)	: 2 Hz/185 kHz
POLARITY	[4] : INVERTED
SIGNAL	[4] : DATA
EQU	[4] : $\sqrt{F}$
Bit rate	: 139 264 kbit/s
Code	: CMI
Nominal amplitude	: 0.1 Vp

Oscilloscope: AC coupling, 50 Ω

Instrument settings:

PJM-4 : (in addition to Section 8.4)

EQUALIZATION	[4]	: FLAT

SNA-1 :

SEND LEVL		: 0 dBm
MENU	[30]	: SPECTRUM ANALYSIS
Centre frequency/FCENT		: 70 MHz
Frequency span/FSPAN		: 0 Hz
REFERENCE		: + 2 dBm
SCALE		: 10 dB
Others/RBW, VBW, INPUT ATT		: AUTO ON

Use the attenuation set to set a basic attenuation of 12 dB and mark the measured trace on the screen on the SNA-1 with the cursor. Change the UUT to $\sqrt{F}$ equalization (EQU [4]). Increase the attenuation by 12 dB with the attenuation set; the measured trace should remain roughly constant (typically + 0.5/- 2 dB).

8.5 SYNCHRONIZATION, COUNTING MODE

Instruments required:

1 Spectrum analyzer	SNA-1	from W & G
1 Jitter generator	PJG-4	from W & G
1 Test probe	TK-11	from W & G

8.5.1 SYNCHRONIZATION

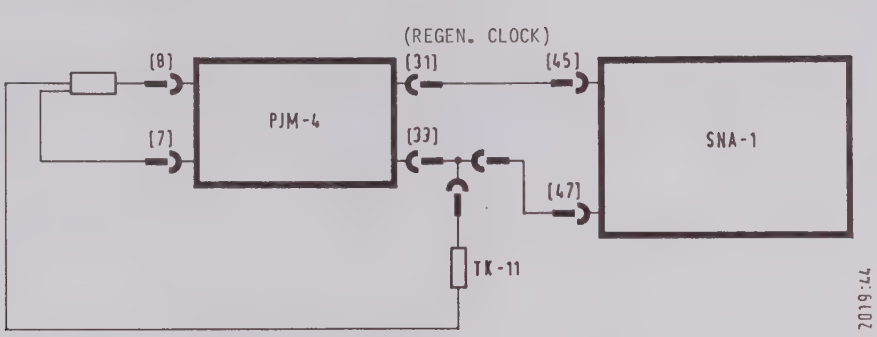


Fig. 8.5-1 Test setup for testing synchronization

Instrument settings:

PJM-4:

INPUT	[4]: CLOCK
Code	: NRZ/ECL
Filter	: CCITT/LP+HP1

SNA-1:

Menu	[30]: 2 (NETWORK A.)
FSPAN	[39]: 0
REFERENCE	: + 2.5 dB
SCALE	: 25 dB
SEND. LEVL	[32]: 0 dBm
RBW; SWT	: 3 Hz; 0.5 s

Make the other settings as shown in the Table below. The PJM-4 should synchronize at each setting.

Bit rate kbit/s PJM-4	Specified error limit (e)	Frequency [kHz] SNA-1	
2048	+ 75 ppm	2048, 154	± 75 ppm is valid for
8448	+ 75 ppm	8448, 634	all other bit rates.
25776	+ 75 ppm	25777, 933	
34368	+ 75 ppm	34370, 578	Test setup error
139264	+ 75 ppm	139274, 445	(m): negligible
2048	- 75 ppm	2047, 846	
8448	- 75 ppm	8447, 366	
25776	- 75 ppm	25774, 067	
34368	- 75 ppm	34365, 422	
139264	- 75 ppm	139253, 555	
Bit rate kbit/s PJM-4	Specified error limit (e)	Frequency [kHz] SNA-1	
External series A, B*	8 MHz	8000	* If option 2019/00.12 is
External series C...	0.7 MHz	700	fitted, the specifications of series C... apply
External	168 MHz	168,000	

Figure 8.5-2 Table for testing synchronization

8.5.2 COUNTING MODE

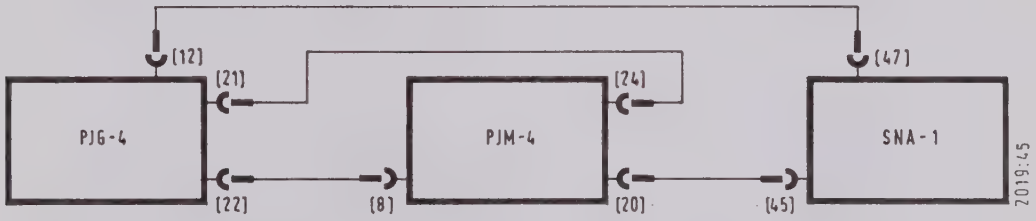


Fig. 8.5-2 Test setup for counting mode

Instrument settings:

PJM-4:

INPUT	[4]:	CLOCK
Code	:	NRZ/TTL
Filter	:	LP 1200 kHz
		HP 20 Hz
Bit rate	:	8448 kbit/s
CODE ERROR	:	EXTERNAL
GATING	:	1 s
COUNT STATUS	:	REP.
PHASE HITS/THRESHOLD	:	ON/0.1 UI_p
JITTER	:	+ p
Code viol. input/EXT.	[22]:	TTL/10 kΩ

PJG-4:

CLOCK	[4]:	INTERNAL
BIT RATE	[1]:	8448 kbit/s
JITTER	[5], [6], [7]:	1.00 UI_{pp}
MODULATION	[13]:	EXTERNAL
PATTERN	[15]:	1 ... 16
DIGITAL WORD	[16], [17], [18]:	11111000000 (5 x "1", 6 x "0")
CODE	[19]:	NRZ/TTL
Clock	[20]:	TTL

SNA-1:

SEND LEVL	[32]:	0 dBm
Menu	[30]:	1 (SPECTRUM)
SCALE	:	50 dB
REFERENCE	[38]:	0 dBm
FSPAN	[39]:	50 Hz
FCENT	[32]:	768.000 kHz
RBW, SWT	:	AUTO ON

Switch off modulation [13] on the PJG-4. Use the vertical cursor on the SNA-1 to determine the counter starting frequency (cursor set to maximum [4]). Enter the frequency thus found as the new FCENT value and set FSPAN to 0 Hz.
Switch on EXTERNAL modulation ([13]) on the PJG-4 and start counting on the PJM-4 ([6]). Read the PHASE HITS and CODE ERROR counting results. (If they differ by more than 1 digit, correct the SNA-1 centre frequency as before).
Form the difference between the counting result and the value on the centre frequency display (in Hz on the SNA-1) and compare it with the error limit.

Specified error limit (e): $\pm$ 38.4 Hz (or dig.)
Test setup error (m) : $\pm$ 1.1 Hz (or dig.)

8.6 JITTER MEASURING ACCURACY

Instruments required:

1 Spectrum analyzer	SNA-1	from W & G
1 Jitter generator	PJG-4	from W & G
1 Selective level meter	SPM-19	from W & G
1 Level generator	PS-19	from W & G
1 T-adapter, 2 x 75 Ω	BN 595/01	from W & G

8.6.1 BASIC NOISE

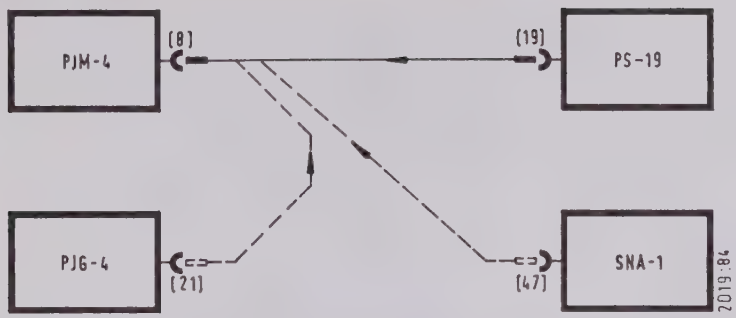


Fig. 8.6-1 Test setup for measuring the basic noise

Instrument settings:

PJM-4:

INPUT	[4]: CLOCK
Code	: NRZ/ECL
Filter	: MAN., HP 2Hz
Result	: JITTER PP, AVERAGE

PS-19:

Level	[6], [13]: 0 dB
Impedance	[15]: 75 Ω

SNA-1:

Menu	[30]: 2 (NETWORK A.)
FSPAN	[39]: 0
SEND LEVL	[32]: 0 dBm

Make the other settings as per the Table below. Read the settled jitter-measuring result (after 10 display changes) at each bit rate setting.

PJM-4		Frequency			
Bit rate in kbit/s	LP in kHz	PS-19 in kHz	SNA-1 in kHz	Specified error limit (e)	Test setup error (m)
2048	185	2048		Series A,B* 0.010 UI_{pp}	
8448	600	8448		Series C... 0.005 UI_{pp}	0.004 UI_{pp}
25776	600		25776		
34368	1200		34368	Series A,B* 0.020 UI_{pp}	0.006 UI_{pp}
139264	6700		139264	Series C... 0.010 UI_{pp}	

Fig. 8.6-2 Basic noise with clock signal

Note: The above measuring uncertainties are not characteristic data of the instruments used. If the limit values are exceeded, reference measurements should be made with a good synthesizer (e.g. Racall-Dana).

* If option BN 2019/00.12 is fitted, the specifications of series C... apply.

Basic noise with data signal

Settings on the PJG-4	Settings on the PJM-4 and PJG-4	Specified error limit (e)	Test setup error (m)
Pattern: $2^{23}-1$ Mod.: OFF	Code: CMI Bit rate: 139264 kbit/s (LP6: 6.7 MHz on PJM-4)	Series A,B* 0.035 UI_{pp} Series C... +0.028 UI_{pp} -0.012 UI_{pp}	0.040 UI_{pp}

Fig. 8.6-3 Basic noise with data signal

Note: The test setup given here is not suitable for verifying the error limit. However, this method is suitable for establishing the major deviations to be expected in the event of a fault.

* If option BN 2019/00.12 is fitted, the specifications of series C... apply.

8.6.2 JITTER DISPLAY

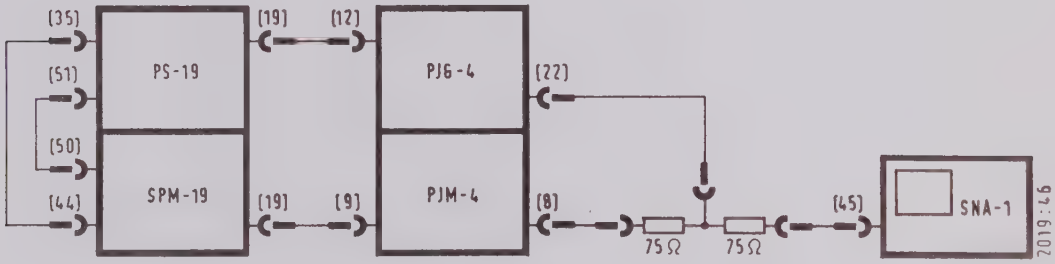


Fig. 8.6-4 Test setup for jitter display

Instrument settings:

PJM-4:

INPUT	[4]: CLOCK
Filter	: MAN
	HIGH-PASS: 10 Hz
	LOW-PASS: 74 kHz
Result	: JITTER PP, AVERAGE

PS-19:

Tuning/EXT.	[7]: ON
Impedance	[15]: 75 Ω

SPM-19:

Bandwidth	[16]: 25 Hz
DISPLAY	[3]: ABS.
MODE	[4]: DGTL
Averaging/AVRG	[11]: ON

PJG-4:

CLOCK [4]: INTERNAL
Modulation [13]: EXTERNAL
Mod. deg./JITTER UI_{pp} [5], [6], [7]: 1.00

SNA-1:

MODE MENU [30]: SPECTRUM ANALYSIS
Others/VBW, SWT, INPUT ATT : AUTO ON

8.6.2.1 Absolute display at various bit rates

Instrument settings (in addition to Section 8.6.2):

PJM-4:

Code : NRZ/ECL

PS-19:

Level [6], [13]: approx. -7 dB

SPM-19:

Frequency [7], [12]: 1 kHz

PJG-4:

Code [20], [19]: NRZ/ECL

SNA-1:

SCALE : 2.5 dB
Bandwidth/RBW : 30 Hz
FSPAN [32]: 2500 Hz
REFERENCE [38]: approx. -7 dBm

Consecutively set each built-in bit rate simultaneously on the PJM-4 and PJG-4. Tune the centre frequency of the SNA-1 (FCENT) exactly to the carrier line (to do so, set "MOD. OFF" on PJG-4 [14]). Then set the level of the auxiliary generator (PS-19) in such a way as to obtain the smallest possible difference between the carrier and the first-order side lines on the SNA-1 (< 0.1 dB). After each measurement, read the settled jitter-measuring result on the UUT and the demodulated level on the SPM-19.

Bit rate range	Required value ± error limit (e)	Test setup error (m)
≤ 30 Mbit/s	0.457 ± 0.033 UI_{pp} or -32.82 ± 0.63 dB	+ 0.008 UI_{pp}
> 30 Mbit/s	0.457 ± 0.043 UI_{pp} or -32.82 ± 0.82 dB	- 0.0 or ± 0.15 dB

8.6.2.2 Display linearity

Instrument settings (in addition to Section 8.6.2):

PJM-4:

Code : NRZ/TTL
Bit rate : 34368 kbit/s

PJG-4:

Bit rate [1]: 34368 kbit/s
Code [19], [20]: NRZ/TTL

SNA-1:

SCALE	: 50 dB
Bandwidth/RBW	: 30 Hz
Frequency span/FSPAN	[32]: 200 Hz
REFERENCE	[38]: approx. +5 dBm

SPM-19:

Frequency	[7], [12]: 1 kHz

PS-19:

Level	[6], [13]: approx. 0 dB

Tune the centre frequency FCENT [35] on the SNA-1 in such a way that the carrier line is positioned at the centre of the screen (approx. 34368 kHz). Then adjust the PS-19 send level until the carrier amplitude reaches a minimum (< -30 dB). Now read the settled jitter-measuring result on the UUT and the demodulated level on the SPM-19 and compare them with the required values. Perform the measurement at every setting given in the Table.

PJG-4 [5], [6], [7]	Required value ± error limit (e) on the PJM-4	on the SPM-19	Test setup error (m) Series A,B*	Series C...
0.76 UI_{pp}	0.765 ± 0.058 UI_{pp}	- 28.34 ± 0.64 dB	+ 0.010 / - 0.002 UI/± 0.15 dB	± 0.006 UI/± 0.15 dB
1.76	1.757 ± 0.108	- 21.12 ± 0.52	+ 0.015 / - 0.007 / -"-	± 0.011 / -"-
2.7	2.75 ± 0.16	- 17.21 ± 0.48	± 0.02 / -"-	± 0.02 / -"-
3.7	3.75 ± 0.21	- 14.53 ± 0.47	± 0.03 / -"-	± 0.03 / -"-
4.7	4.75 ± 0.26	- 12.48 ± 0.46		
5.7	5.75 ± 0.31	- 10.82 ± 0.45	± 0.04 / -"-	± 0.04 / -"-
6.7	6.75 ± 0.36	- 9.43 -"-		
7.7	7.75 ± 0.41	- 8.23 -"-	± 0.05 / -"-	± 0.05 / -"-
8.7	8.75 ± 0.46	- 7.18 ± 0.44		
9.7	9.75 ± 0.51	- 6.24 -"-	± 0.06 / -"-	± 0.06 / -"-
10.7	10.75 ± 0.56	- 5.39 -"-		
11.7	11.75 ± 0.61	- 4.62 -"-	± 0.07 / -"-	± 0.07 / -"-
12.7	12.75 ± 0.66	- 3.91 -"-		
13.7	13.75 ± 0.71	- 3.25 -"-	± 0.08 / -"-	± 0.08 / -"-
14.7	14.75 ± 0.76	- 2.64 -"-	± 0.09 / -"-	± 0.09 / -"-
15.7	15.75 ± 0.81	- 2.07 -"-		

Fig. 8.6-5 Table for the linearity test

* If option BN 2019/00.12 is fitted, the specifications of series C... apply.

8.6.2.3 Display frequency response

Instrument settings (in addition to Section 8.6.2):

PJM-4:

Code : NRZ/ECL
Filter : MAN
HIGH-PASS: 2 Hz

PJG-4:

Code [20], [19]: NRZ/ECL

PS-19:

Level [6], [13]: approx. -7 dB

SNA-1:

SCALE : 2.5 dB
Bandwidth/RBW : AUTO ON
REFERENCE [38]: approx. -7 dBm

Reference measurements

At each bit rate, first determine the reference value for the frequency measurement at 1 kHz modulation frequency. First tune the centre frequency of the SNA-1 (FCENT) exactly to the carrier line, then adjust the level of the modulation generator (PS-19) in such a way that the smallest possible difference is obtained between the carrier and the first-order side lines on the SNA-1 (< 0.1 dB). Read the measured values on the UUT and on the SPM-19, correct them as follows and use them as reference values for evaluating the frequency response.

Reference value = Reading + Corr.

$$\frac{\text{Corr.}}{UI_{pp}} = \left(\text{Carrier} - \frac{\text{1st side line right} + \text{1st side line left}}{2}\right) \cdot \frac{1}{1.8} \cdot 0.05$$

$$\text{or } \frac{\text{Corr.}}{\text{dB}} = \left(\text{Carrier} - \frac{\text{1st side line right} + \text{1st side line left}}{2}\right) \cdot \frac{1}{1.8}$$

Bit rate [kbit/s] PJG 4, PJM 4	f_{mod} [kHz] SPM 19	Low-pass/LP [kHz] PJM 4	Specified error limit (e) [UI_{pp}] or [dB]	
2048	1 (reference)	600	---	---
	10		0.009	0.17
	40		0.018	0.35
	50			
	70			
	100			
8448	1 (reference)	1200	---	---
	100		0.018	0.35
	200		-"-	-"-
	400		0.023	0.44
25776	1 (reference)	1200	---	---
	100		0.018	0.35
	200		-"-	-"-
	400		0.023	0.44
	800		-"-	-"-
34368	1 (reference)	6700	---	---
	100		0.018	0.35
	400		0.023	0.44
	800		-"-	-"-
139264	1 (reference)	6700	---	---
	0.12		0.009	0.17
	10		-"-	-"-
	100		0.018	0.35
	200			
	300			
	500		0.023	0.44
	1000		-"-	-"-
	3000		0.031	+ 0.59 / - 0.63
	4500		0.045	+ 0.83 / - 0.92

Fig. 8.6-6 Table for testing the frequency response

Measurements

Set the modulation frequency in accordance with the Table (Fig. 8.6-6) and enter a frequency span (FSPAN) of 2.5 . f_{mod} on the SNA-1 [32]. Set the auxiliary level, read off the results and calculate the correction value in the manner described for the reference measurement. Then calculate the difference from the reference value (after correcting the measured value with the associated correction value!) and compare it with the error limit (e).

Test setup error (m): $\pm$ 0.002 UI_{pp}

or: $\pm$ 0.09 dB

Example:

Measured value: 0.483 UI_{pp} or -32.42 dB

L on SNA-1: -0.07 dB (cursor on carrier, rel. cursor on side lines Display REL: 0.07 dB

Corr.: (-0.07 dB) . $\frac{1}{1.8}$ = - 0.04 dB or -0.04 dB 0.05 $\frac{UI}{dB}$ = - 0.002 UI

Measured value, corr. : 0.481 UI_{pp} or -32.46 dB

Reference value, corr. : 0.478 UI_{pp} or -32.52 dB

Difference : 0.003 UI_{pp} or +0.06 dB

9 FUNCTIONAL AND CIRCUITRY DESCRIPTION 9-1

9.1 Functional description 9-1
9.1.1 Functional description of the overall PJM-4 instrument 9-1
9.1.2 Function-related clock circuit diagram 9-6
9.1.3 Instrument synchronization 9-9
9.1.3.1 Principle of instrument synchronization 9-9
9.1.3.2 Status diagrams for the synchronization sequence 9-15
9.1.3.3 Setting tables for control circuits 9-18

9.2 Circuitry descriptions 9-19
9.2.1 Frequency generator (A) 9-19
9.2.1.1 Carrier oscillator [5/2019-P] 9-19
9.2.1.2 Carrier phase meter [6/2019-Q] 9-20
9.2.1.3 Lock-in oscillator [6/2019-R] 9-22
9.2.1.4 Clock divider [6/2019-S] 9-23
9.2.2 Input circuit (B) [2/2019-V] 9-23
9.2.2.1 Signal path 9-23
9.2.2.2 Peak rectifier 9-24
9.2.2.3 Zero-point control 9-24
9.2.2.4 Threshold switching 9-24
9.2.2.5 Equalizer mode ($\sqrt{f}$) 9-25
9.2.3. Code error (C) 9-25
9.2.3.1 Code error 1 [3/2019-AL] 9-25
9.2.3.1.1 "Delay correction" function block 9-25
9.2.3.1.2 "Clock inverter/Driver" function block 9-27
9.2.3.1.3 "Data receiver" function block 9-27
9.2.3.1.4 "Data sampler" function block 9-27
9.2.3.1.5 "CMI detector" function block 9-28
9.2.3.1.6 "AMI/HDB-3 detector" function block 9-31
9.2.3.1.7 "External code error input" function block 9-37
9.2.3.1.8 "Multiplexer" function block 9-37
9.2.3.1.9 "Rear panel buffer stage" function block 9-37
9.2.3.1.10 "Error counter" function block 9-37
9.2.3.1.11 "AIS counter" function block 9-38
9.2.3.1.12 "Memory, address decoder, pulse shaper" function block 9-38
9.2.3.2 Code error 2 [Option] [4/2019-A0] 9-38
9.2.3.2.1 "Data receiver" function block 9-39
9.2.3.2.2 "Delay compensation/Data sampler" function block 9-39
9.2.3.2.3 "Error detector" function block 9-40
9.2.4 220 MHz circuit (D) 9-46
9.2.4.1 220 MHz VCO [7/2019-M] 9-46
9.2.4.2 Controller 2 [7/2019-N] 9-46
9.2.4.3 Sawtooth phase meter (STPM) [7/2019-O] 9-49
9.2.4.4 170 MHz low-pass filter [7/2019-T] 9-51
9.2.4.5 Mixer [7/2019-U] 9-52
9.2.4.6 Buffer stage 2 [7/2019-W] 9-52
9.2.5 11 MHz circuit (E) 9-52
9.2.5.1 11 MHz phase meter [8/2019-G] 9-52
9.2.5.2 Controller 1 [8/2019-H] 9-54
9.2.5.3 11 MHz VCO [8/2019-J] 9-56
9.2.5.4 20:1 divider [8/2019-AM] 9-57
9.2.5.5 11 MHz filter [8/2019-AN] 9-57
9.2.6 Adder (F) [10/2019-AF] 9-57
9.2.7 Filter (H) [11/2019-Y] 9-59
9.2.7.1 Block circuit diagram 9-59
9.2.7.2 Selectable low-pass filters 9-59
9.2.7.3 Selectable high-pass filters 9-59
9.2.7.4 External filter 9-63
9.2.7.5 4.5 MHz low-pass, 1.83 Hz high-pass 9-63
9.2.7.6 Demodulator output 9-63
9.2.7.7 Address decoder, transceiver 9-63
9.2.7.8 Buffer amplifier; external amplifier 9-64
9.2.8 Peak rectifier (K) [12/2019-Z] 9-64
9.2.8.1 Block circuit diagram (see Fig. 9.2-37) 9-64
9.2.8.2 30 dB amplifier [12/2019-AH], hit counter amplifier [12/2019-AJ], peak rectifier amplifier [12/2019-AG] 9-67
9.2.8.3 Peak value meters, overload monitor 9-67
9.2.8.4 Holding element 9-68
9.2.8.5 Pulse generator 9-69
9.2.8.6 A/D conversion 9-69
9.2.8.7 Divider controller 9-71
9.2.8.8 Hit counter amplifier, 30 dB amplifier, peak rectifier amplifier 9-72
9.2.8.9 -20 dB, -10 dB divider 9-72
9.2.8.10 1/16, 1/4 divider 9-72
9.2.8.11 Voltage supply 9-72

9.2.9 Hit counter (I) [13/2019-AA] ... 9-73
9.2.10 RF control (G) [14/2019-F] ... 9-73
9.2.11 Display/control section (L) ... 9-75
9.2.11.1 Display ... 9-75
9.2.11.2 Keyboard [16/2019-A] ... 9-80
9.2.12 Power supply unit (N) ... 9-81
9.2.12.1 Functional description of the power supply unit ... 9-81
9.2.12.2 Circuitry description by functional groups ... 9-82
9.2.13 Description of the professor card CPU-2, BN 965, circuit diagram (90) ... 9-87
9.2.13.1 Reset and mains OFF function ... 9-87
9.2.13.2 Clock generation ... 9-87
9.2.13.3 Latches, drivers and memories ... 9-88
9.2.13.4 Control lines ... 9-88
9.2.13.5 Data-save ... 9-89
9.2.13.6 Demultiplexer IC 2 ... 9-90
9.2.13.7 Free-running ... 9-91
9.2.13.8 IO bus ... 9-91
9.2.13.9 IO timing control ... 9-92
9.2.13.10 Test points ... 9-95
9.2.13.11 Bank switching ... 9-95
9.2.14 IEEE 488 / <IEC 625> Interface bus card, BN 958, circuit diagram (91) ... 9-95
9.2.14.1 Functional description based on the block circuit diagram ... 9-95
9.2.14.2 Functional description of the card ... 9-97
9.2.14.3 Structure of the IEC bus program ... 9-99

9.3 Software description ... 9-100
9.3.2 Description of "ENTW" test menu ... 9-104
9.3.3 Self test menu "TEST" ... 9-105
9.3.4 Monitor program "SERVICE" (WORIS functions) ... 9-105
9.3.5 Cyclic hardware repair programs ... 9-107

9 FUNCTIONAL AND CIRCUITRY DESCRIPTION

9.1 FUNCTIONAL DESCRIPTION

9.1.1 FUNCTIONAL DESCRIPTION OF THE OVERALL PJM-4 INSTRUMENT

The description is based on the block circuit diagrams in Fig. 9.1-2, Part 1 + 2. The individual function blocks are marked (A), (B), etc. Circuits are assigned to function blocks only on the basis of their functional relationship, not in accordance with the position of the individual circuits in the instrument or on the circuit boards.

Jitter measurement:

Input section (B):

The input signal (clock/data) is first conditioned in input section (B) and then passed as <DA+> or <DA-> signal to Code error detector (C), and as a pulse signal to Phase meter 1 (sawtooth phase meter) in the first PLL, the 220 MHz circuit (D). The pulse signal supplied contains the full phase jitter (Je) of the input signal.

220 MHz circuit (D):

Phase meter 1 always operates at the bit rate frequency and, due to its S & H behaviour, can also process input signals with missing edges (data signals). While it is part of the first PLL, it also lies in the measuring branch and its output signal is part of the measured jitter.

The 220 MHz circuit regenerates the clock signal from the jittered pulse signal by converting the frequency of the controlled 220 MHz VCO with the carrier frequency supplied by Frequency generator (A) and derived from internal crystals or the external clock.

The PLL ensures that the clock thus regenerated remains in phase with the input signal. For jitter frequencies below the control limit frequency of the PLL, the regenerated clock provides a true image of the phase jitter of the input signal.

11 MHz circuit (E):

The low-frequency component of the phase jitter (Jreg) regulated into the 220 MHz circuit is divided by 20 and then measured by Phase meter 2 (11 MHz phase meter) as J_{11} in a second PLL, the 11 MHz circuit.

Adder (F):

The higher-frequency components of the phase jitter, which the 220 MHz circuit can no longer follow, are measured only by the sawtooth phase meter (high-pass behaviour); the low-frequency components, which the 220 MHz circuit follows, are detected by the 11 MHz phase meter (low-pass behaviour).

The addition of the two phase meter signals with correct amplitude and phase in the adder yields the demodulated jitter of the input signal over the entire measuring bandwidth (also see Fig. 9.1-1).

The high and low-pass limit frequencies of the two measuring branches are equal to the control limit frequency of the 220 MHz circuit.
The modulation capacity of the sawtooth phase meter applies as the measuring range for frequencies above the control limit frequency.

For frequencies below the control limit frequency, the 20:1 division in the 11 MHz circuit results in a measuring range up to 20 times greater, provided that the loop gain in the 220 MHz circuit for the associated frequency components is sufficient to regulate the phase jitter into the circuit to such an extent that the residual modulation on the sawtooth phase meter does not exceed its modulation capacity.

Frequency generator (A):

The frequency generator provides the carrier frequency f_T. The carrier frequency is derived from built-in crystals for the fixed bit rates provided in the instrument. In this case, the following applies:

$$f_T = f_{bit\ rate} + 220\ MHz$$

If the carrier frequency is derived from an external clock, the following applies:

$$f_T = f_{ext.\ clock} + 220\ MHz$$

Code error (C):

The code error circuit checks the received data signal for coding errors. To do so, the DA+ and DA- signal arriving from the input circuit is sampled with the regenerated clock.
Since this sampling clock must be in phase quadrature in relation to the regenerated clock in the 220 MHz circuit, it is generated in a separate mixer/LP circuit with the frequency of the 220 MHz VCO, which is in phase quadrature.
The code errors occurring are counted and passed to the processor section for evaluation.
The 10 Hz counting clock is supplied by the peak rectifier circuit.

RF control:

The RF control (G) handles control of the RF assembly, comprising the following:

Frequency generator (A)
Input section (B)
Mixer and LP filter for Code error (C)
220 MHz circuit (D)
11 MHz circuit (E)
Adder (F)

It decodes digital control signals for the RF assembly and passes on status information to the processor section. D/A converters generate the analog control signals.

Simplified representation of the jitter meter function:

Je : Jitter of the input signal
J_{reg} : Jitter of the generated clock (regulated jitter)
U_{220} : Output signal, Phase meter 1 (sawtooth phase meter)
U_{11} : Output signal, Phase meter 2 (11 MHz phase meter)
Ua : Demodulated jitter signal

Where : $U_{220} \sim J_e - J_{reg}$

$U_{11} \sim J_{reg/20}$

For addition, this thus yields:

$$U_a \sim J_e$$

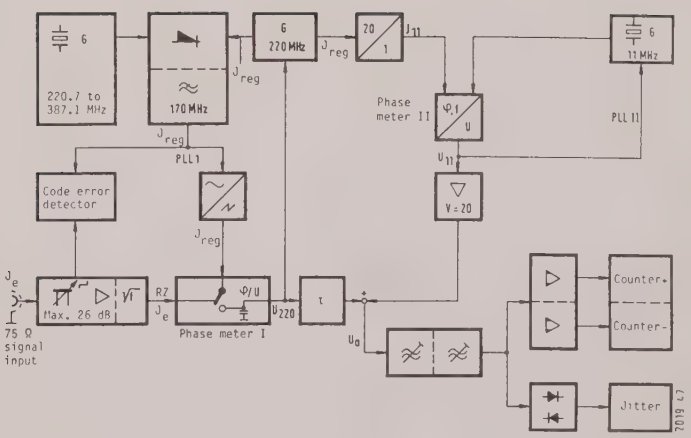


Fig. 9.1-1 Simplified representation of the jitter meter function

Jitter evaluation:

Filter (H):

The demodulated jitter signal arriving from the adder passes through selectable internal or external filters in the filter section and is available at the demodulator output for further external evaluation.

Peak rectifier (K):

The peak rectifier amplifies the filtered jitter signal as a function of level and measures the positive and negative peak values with an A/D converter.
The resultant measurement is processed in the processor section (L) and displayed.
A crystal-stabilized 10 Hz generator supplies the clock signal for the A/D converter and the hit counter.

Hit counter (I):

The hit counter (I) detects positive and negative transgressions of a selectable threshold value by the jitter signal, counts them and passes them on to the processor section for further evaluation.

9.1.2 FUNCTION-RELATED CLOCK CIRCUIT DIAGRAM

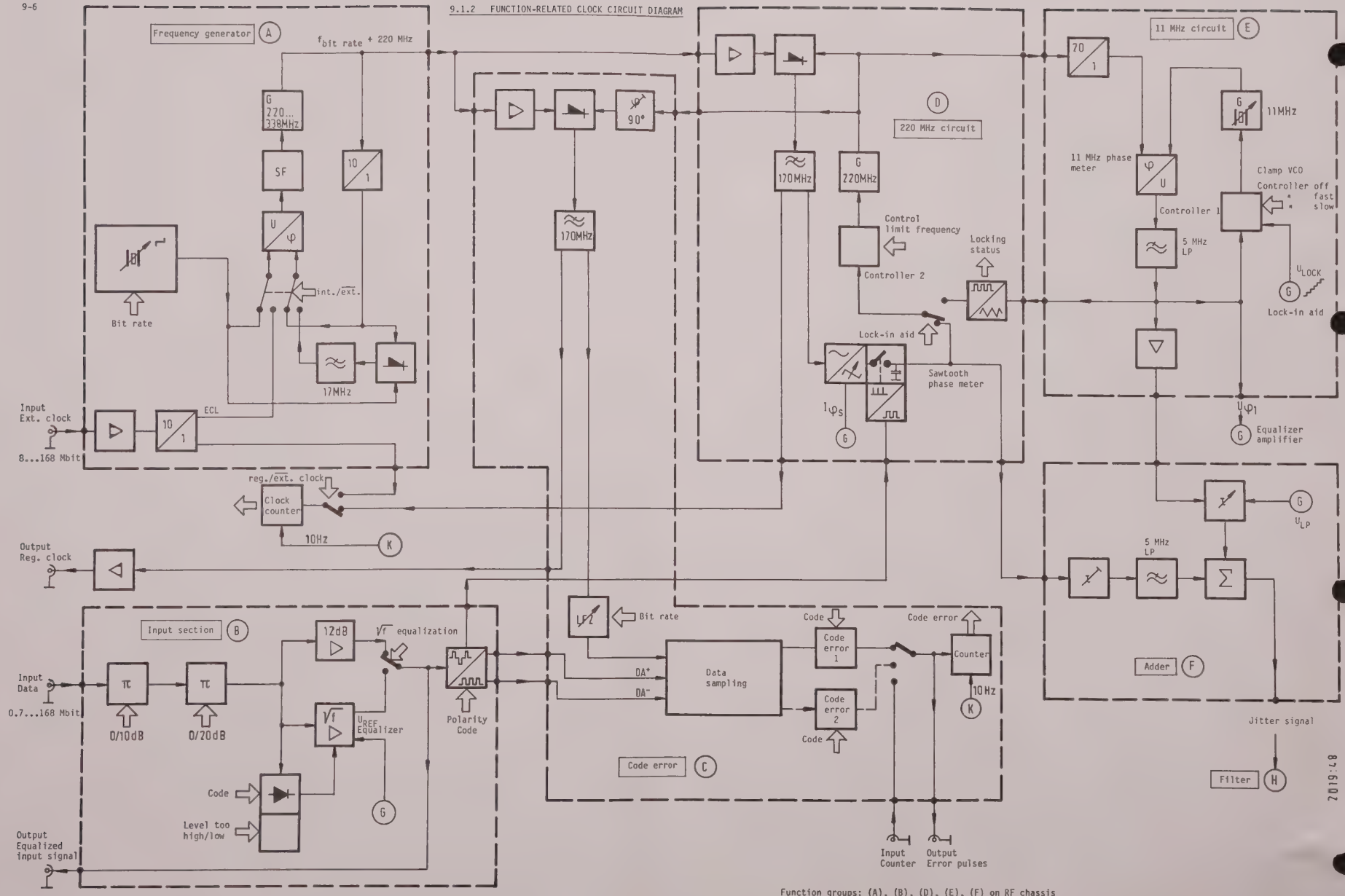


Fig. 9.1-2 Simplified block circuit diagram, Part 1

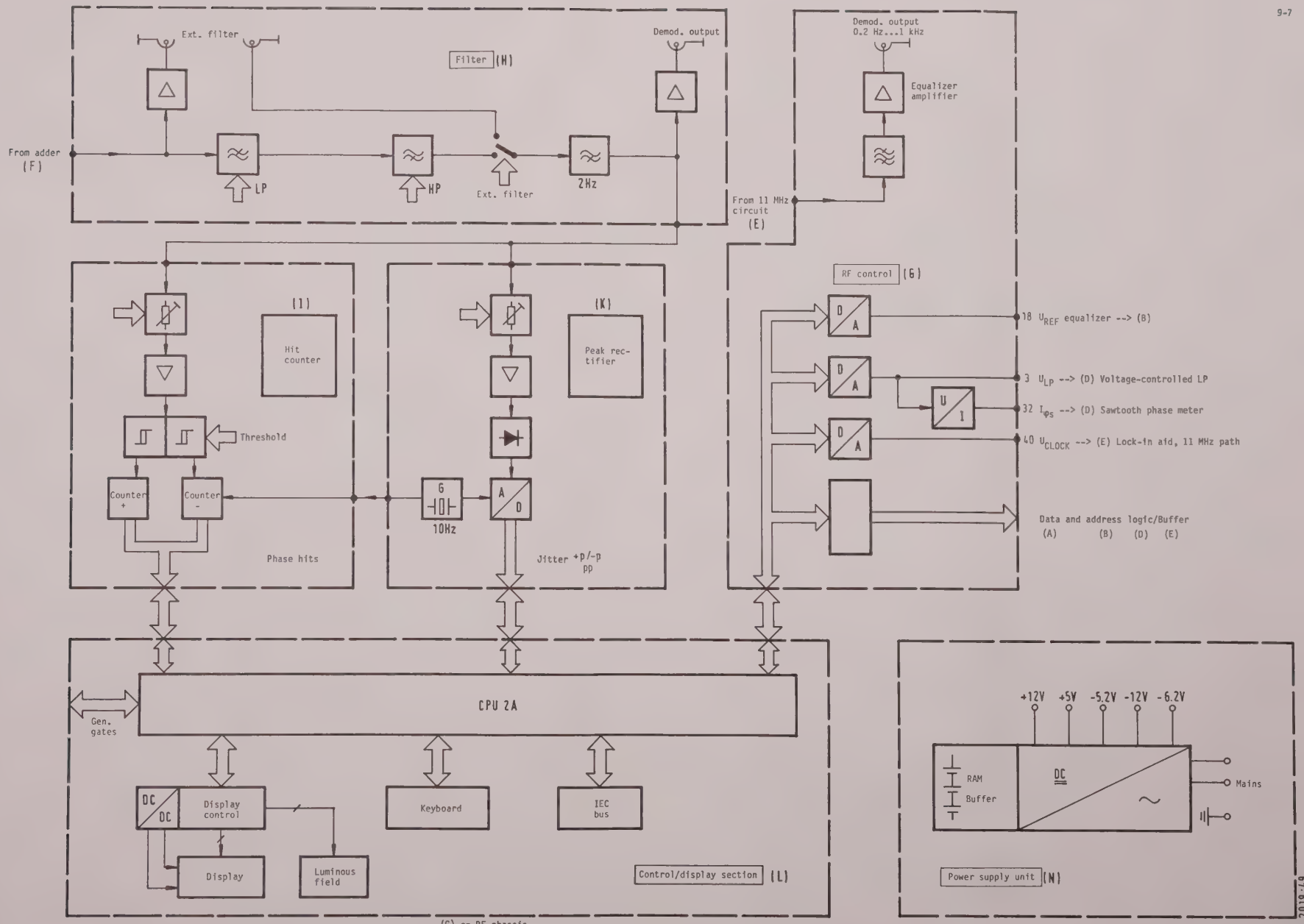


Fig. 9.1-2 Simplified block circuit diagram, Part 2 (H) (I) (K) (L): p.c.b.s

9.1.3 INSTRUMENT SYNCHRONIZATION

9.1.3.1 Principle of instrument synchronization

Introduction:

The two PLLs in the instrument must be synchronized with the input signal. The 220 MHz loop is locked directly onto the input signal and the 11 MHz loop onto the previously locked 220 MHz loop.
Lock-in aids and lock-in checks are provided for both circuits.

Lock-in detection/lock-in monitoring:

Lock-in checks are provided for both circuits for detecting locking during the synchronization process and for monitoring locking during the measuring cycle.

220 MHz circ.: The regenerated clock frequency is constantly measured by a frequency counter (indirect lock-in check).
If the frequency deviation exceeds a limit value, a new lock-in process is initiated.

Limit values: Bit rate > 100 MHz: fg = 20 kHz
Bit rate < 100 MHz: fg = 10 kHz

11 MHz circ. : When unlocked, the 11 MHz phase meter supplies a sawtooth oscillation.
A lock-in aid/lock-in detection circuit, located in Controller 2 (!), checks for the presence of such a sawtooth oscillation.
The phase meter output signal is differentiated for this purpose. The kick-back pulses generated from a sawtooth oscillation set a lock-in FF on the RF control.
The processor polls the lock-in FF cyclically, initiates the necessary lock-in process and resets the lock-in FF.

Lock-in aids:

Both PLLs require lock-in aids for synchronization, since the phase meters used do not have a frequency-sensitive response.
When the circuits are unlocked, both phase meters supply a sawtooth oscillation as output signal which, under ideal circumstances, should have no average. However, the PI controllers cannot derive a directional voltage for the VCOs from this signal, meaning that the slight offset voltages always present in the controllers or phase meters would drive the control voltages into the "corner".
Synchronization is only possible if the differential frequencies are within the small lock-in ranges of the two PLLs, i.e. if pre-tuning of the 11 MHz and 220 MHz VCO is carried out.
This is the purpose of the lock-in aids.

Lock-in aid, 220 MHz circuit (Fig. 9.1-3):

The "lock-in aid" is always active when

a) no input signal is applied,
b) the 220 MHz circuit is unlocked (i.e. the frequency counter measures an excessive frequency deviation of the regenerated clock).

In case a), the sawtooth phase meter supplies no output signal; in case b), it supplies a sawtooth oscillation whose frequency is equal to the difference between input signal and regenerated clock frequency. In both cases, assuming that the differential frequency is beyond the lock-in range of the PLL, the PI controller in Controller 2 runs into the "corner" and the frequency deviation is maximized. Locking-in is impossible in this situation.

The lock-in aid for the 220 MHz circuit is based on the following consideration:
It must be ensured that, even when not synchronized, the frequency deviation of the regenerated clock from the nominal bit rate frequency is smaller than the lock-in range of the 220 MHz circuit. If an input signal is then applied and the 220 MHz circuit closed, the circuit can lock onto the input frequency, provided that its deviation from the nominal bit rate frequency is within the permissible tolerances.

The 220 MHz circuit is broken in the "Lock-in aid" setting.
The 220 MHz VCO is locked onto the 11 MHz VCO via a lock-in aid circuit in Controller 2; in this case, the VCO is permanently tuned to exactly 11 MHz ("Clamp" Controller 1).

The control loop for the lock-in aid comprises the following:
220 MHz VCO
20:1 divider
11 MHz phase meter
PI controller and lock-in circuit in Controller 2
11 MHz VCO as reference

The lock-in aid circuit has a frequency-sensitive response since, when unlocked, directional loading pulses for the PI controller are generated from the sawtooth oscillation of the 11 MHz phase meter in the lock-in aid circuit, meaning that it always locks, provided that the instrument is functioning correctly.

The deviation of the regenerated clock generated in the "Lock-in aid" setting from the nominal bit rate frequency is equal to the sum of the deviations of the 11 MHz VCO and the frequency generator.
These deviations are in the ppm range.
If an input signal is now applied and the 220 MHz made again, it is ensured that the circuit can automatically lock onto the input frequency.

Lock-in aid, 11 MHz circuit (lock-in DAC) (Fig. 9.1-4):

The essential prerequisite for synchronization of the 11 MHz circuit is that the 220 MHz circuit is already synchronized with the input signal and the bit rate frequency is within the permissible tolerance range of the set nominal bit rate frequency.

In the lock-in aid, a search circuit is superimposed on the 11 MHz circuit when made; this search circuit gradually changes the frequency of the 11 MHz VCO during a search run, until the circuit locks or the frequency deviation is within the lock-in range.

The frequency of the VCO is varied in steps by briefly feeding a staircase auxiliary voltage (lock-in DAC "ON" for 25 ms) into Controller 1, which reloads the PI controller and thus increases the tuning voltage by a corresponding value.

The frequency deviation is checked by the lock-in detection circuit in Controller 2, where the sawtooth oscillations output by the 11 MHz phase meter when unlocked set the lock-in FF. The lock-in FF is polled cyclically by the processor 100 ms after each tuning step and reset, if necessary.

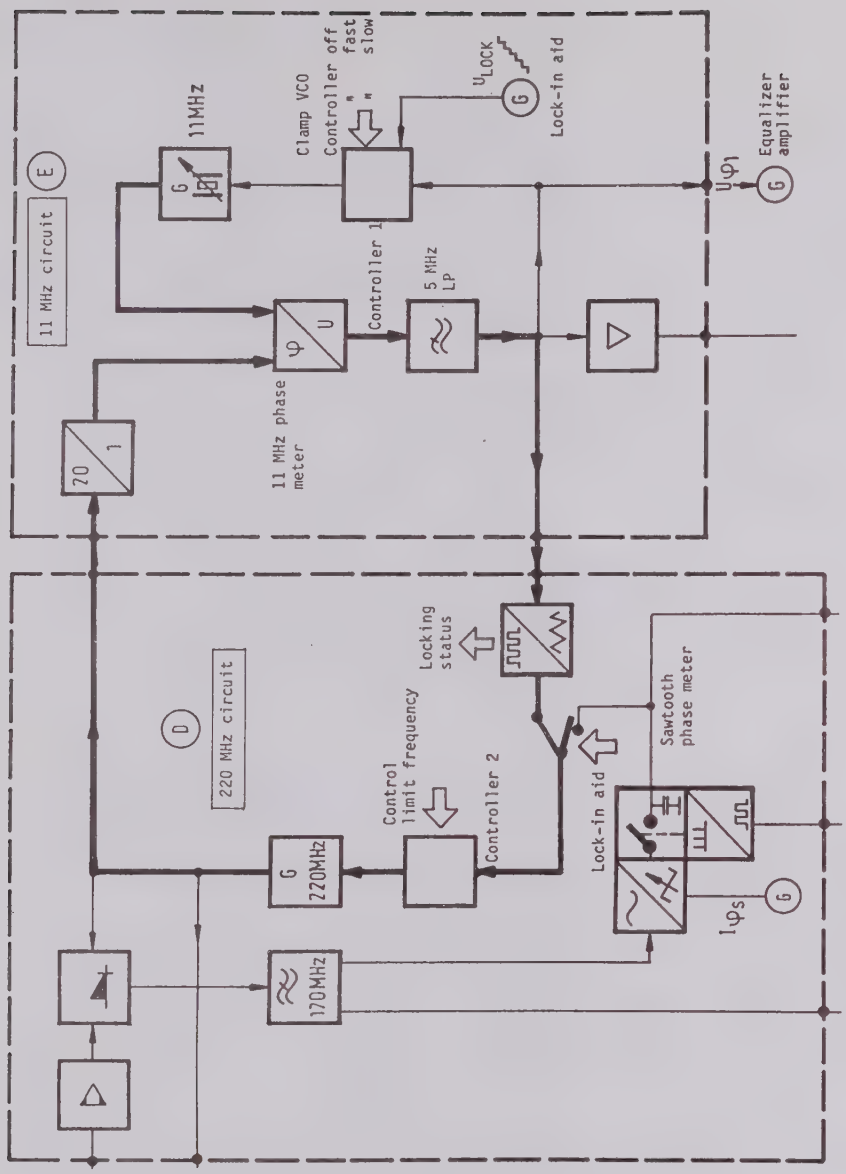
The switch-off criterion for the search run is that the lock-in FF is no longer set between two polling cycles, i.e. the frequency deviation (sawtooth frequency) is smaller than the polling frequency or the cycle has already locked.

The 11 MHz lock-in aid consists of the following:

220 MHz VCO (locked 220 MHz loop)
20:1 divider
11 MHz phase meter
11 MHz VCO
Controller 1 ("fast" on) ; auxiliary voltage fed in at this point
Lock-in detector in Controller 2
Lock-in FF on RF control ; polling and resetting every 100 ms
Lock-in DAC on RF control; generation of auxiliary voltage, increase in steps after each lock-in FF poll

Lock-in sequence:

1. Check whether the 220 MHz circuit is locked (frequency counter).
2. Controller 1 "fast" ON, i.e. increase of the control limit frequency to approx. 100 Hz to enlarge the lock-in range.
3. Search run starts at minimum tuning voltage and stops when the lock-in FF is no longer set. No more than three search runs are performed.
4. Waiting time for the control circuit to settle.
5. Switching to low control limit frequency of approx. 1 Hz (Controller 1 "slow").
6. "Normal" operation achieved (Fig. 9.1-5).



Lock in aid circuit,
220 MHz VCO locked to 11 MHz VCO.

Fig. 9.1-3 Lock-in aid, 220 MHz circuit

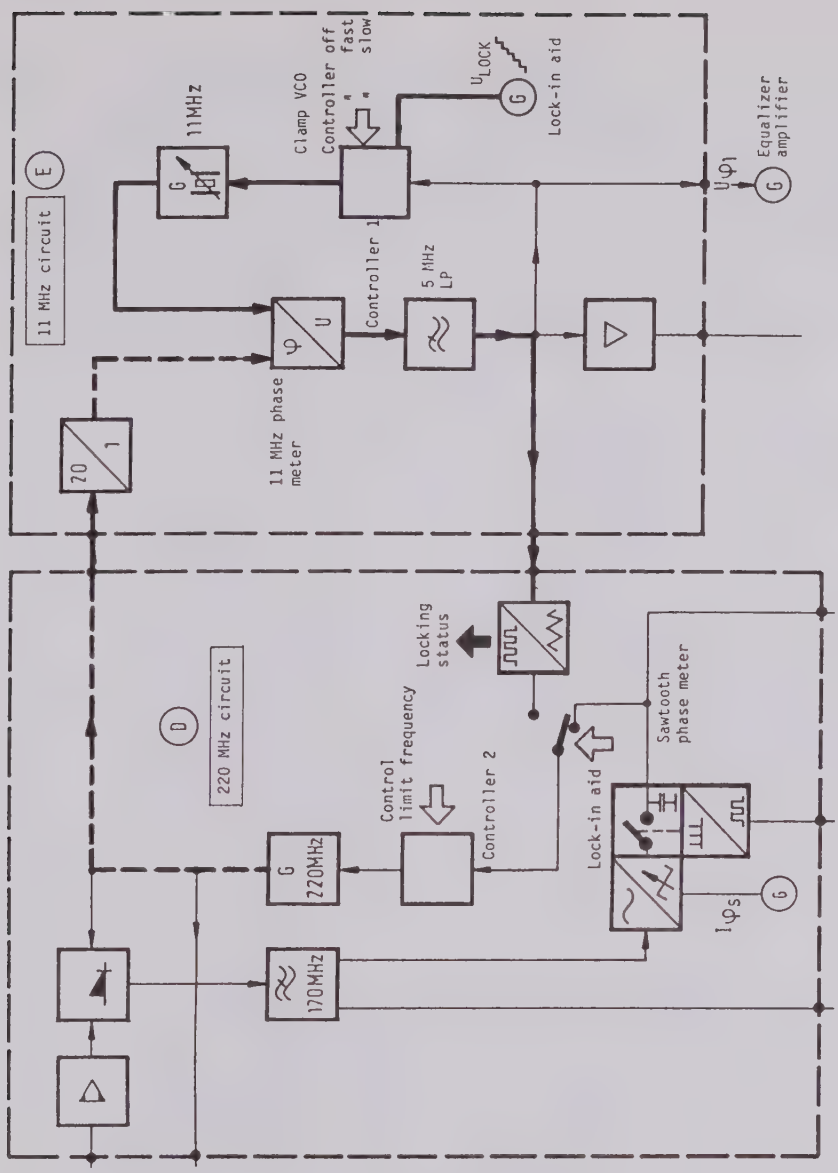


Fig. 9.1-4 11 MHz lock-in aid

220 MHz circuit locked onto input signal (not drawn)

Reference frequency for 11 MHz circuit

11 MHz lock-in aid circuit

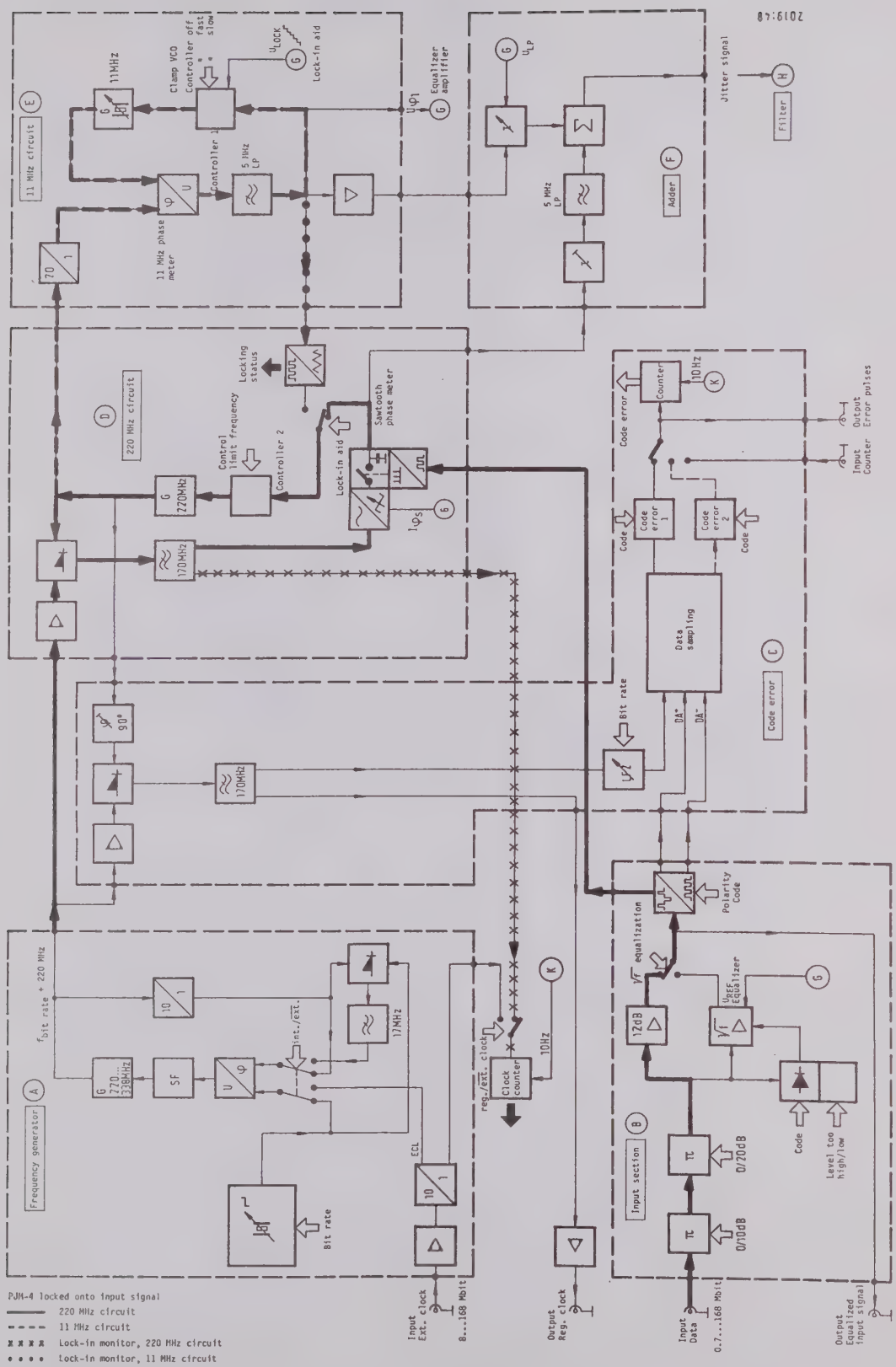


Fig. 9.1-5 Instrument in "normal" mode

9.1.3.2 Status diagrams for the synchronization sequence

The programmed synchronization sequence is described below, starting from the various possible instrument statuses.

Program modules:

The overall sequence can be divided into four functional program modules:

Module (A) : Locking 220 MHz circuit
Module (B) : Locking 11 MHz circuit
Module (C) : Instrument locked normally
Module (D) : Lock frequency generator externally

All control circuit settings and synchronization polls within the modules take place in a 100 ms cycle.

Higher-ranking conditions:

If one of the so-called "higher-ranking conditions" applies at the same time as a poll within a module, the module is exited, regardless of the poll result, and a new start is made at (1) or (2).

A "higher-ranking condition" means that defined re-synchronization has become necessary due to a change in the instrument setting or the input signal.

As long as the "higher-ranking condition" lasts, the module affected (A) or (B) is executed in cyclic form up to the first poll.

The higher-ranking conditions cause:

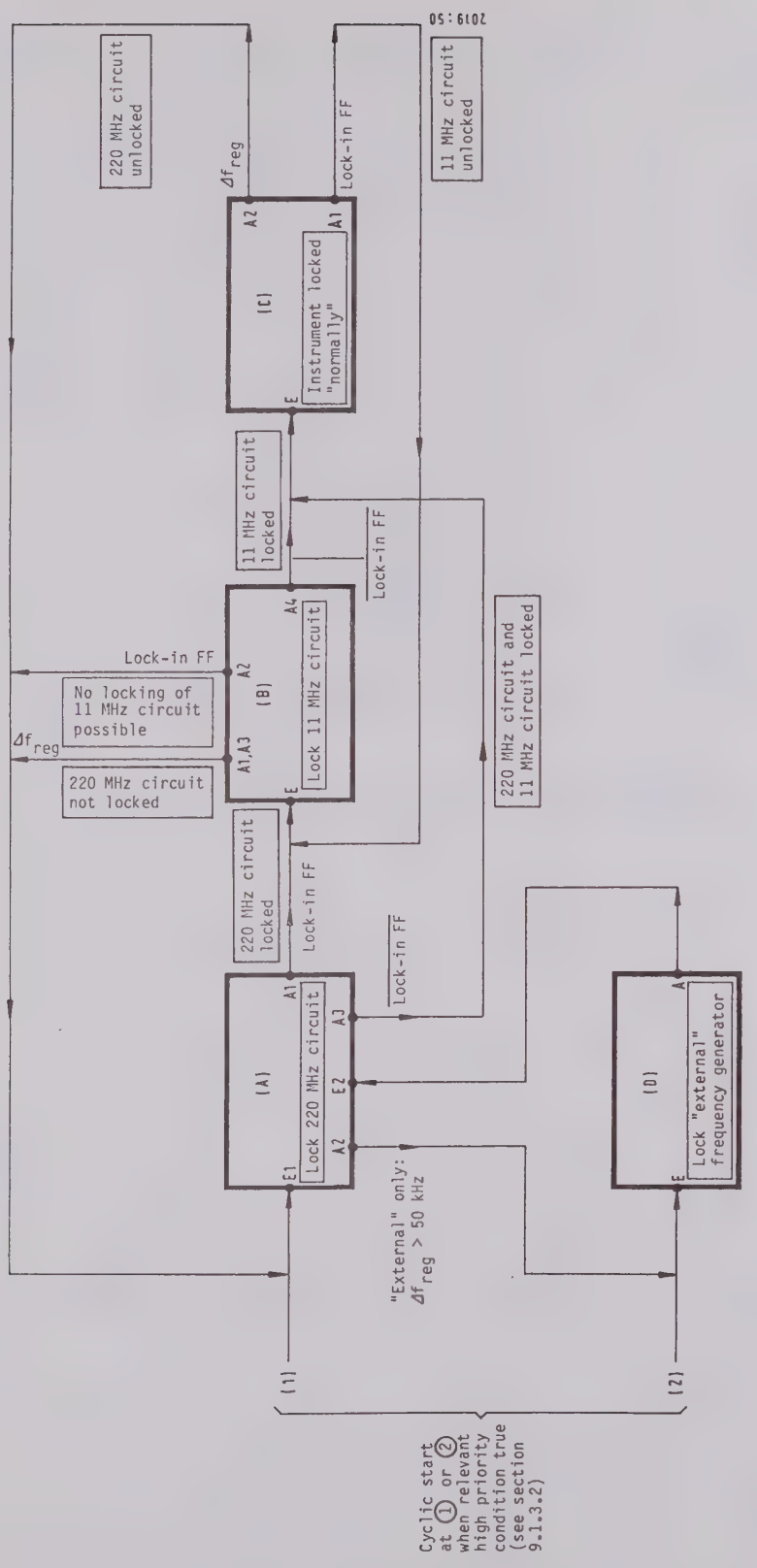
1. Cyclic entry (1) of module (A):

   whenever:
   - no input signal is present
   - a changed instrument setting necessitates re-synchronization
   - the frequency deviation of the regenerated clock is greater than 6 MHz

   only with external clock:
   - when the external clock frequency supplied is less than 8 Mbit or greater than 168 Mbit
   - when switching from status R_EXTERN1 or R_EXTERN2 (module (D)) to internal bit rate

2. Cyclic entry (2) of module (D):

   only with external clock:
   - when the instrument is not locked for longer than 25 ms
   - when the external clock is changed by more than 100 kHz in 200 ms
   - when the frequency deviation of the regenerated clock is greater than 6 MHz



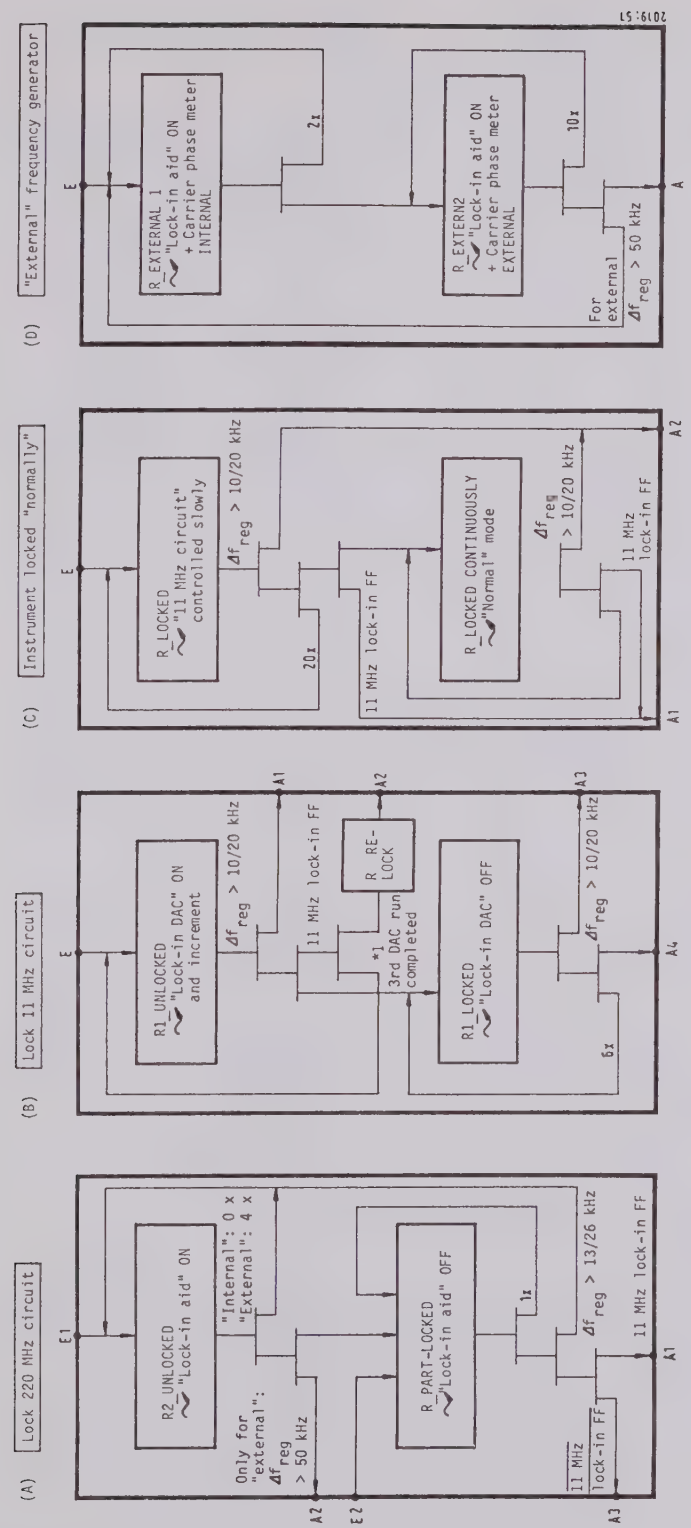
Explanations: Δf_{reg}: Frequency deviation of the regenerated clock greater than the specified limit value, i.e. the 220 MHz circuit is considered to be unlocked.

Lock-in FF/$\overline{\text{Lock-in FF}}$: 11 MHz circuit not locked/locked.

(A),(B),(C),(D): Program modules

①, ②: Starting points for high priority conditions

Fig. 9.1-6 Status diagram for the synchronization sequence



Notes:
* 1 Three DAC search runs follow:
1st run with limited search range and large increment; if 1st run unsuccessful: 2nd and 3rd run with full search range and small increment
- For description of control circuit settings Rx_yyy, see setting tables for control circuits

Δf_{reg}: Frequency deviation of the regenerated clock from the nominal bit rate frequency or the frequencies of the external clock

11 MHz lock-in FF: "1" when 11 MHz circuit not locked

"External/Internal": Operation with internal bit rate frequency/externally applied clock

Functional sequence within program modules (A), (B), (C), (D)
E: Inputs
A: Outputs
See diagram, Part I, for further details

Fig. 9.1-7 Status diagrams for program modules

9.1.3.3 Setting tables for control circuits

1. Control circuit settings: (see Section 9.1.3.2)

Setting	Controller 1		Lock-in DAC	Lock-in aid (Controller 2)	Carrier phase meter
R_PERM. LOCKED	-	-	-	-	-
R2_UNLOCKED	Clamp	Fast	off	on	-
R_PART-LOCKED	Clamp	Fast	off	off	-
R1_UNLOCKED	Free	Fast	on for 15 ms	off	-
R1_LOCKED	Free	Fast	off	off	-
R_LOCKED	Free	Slow	off	off	-
R_EXTERNAL1	Clamp	Fast	off	on	Internal
R_EXTERNAL2	Clamp	Fast	off	on	External

Fig. 9.1-8 Setting table for control circuits

2. Status of controllers and control circuits:

Controller 1: (11 MHz circuit)

- "Clamp" : 11 MHz control circuit interrupted, 11 MHz VCO receives fixed tuning voltage
- "Free" : 11 MHz control loop made
- "Fast" : High control limit frequency of approx. 100 Hz set to extend lock-in range during the lock-in process
- "Slow" : Control limit frequency approx. 1 Hz for "normal" mode

Lock-in DAC: (lock-in aid for 11 MHz circuit)

- "on" : Auxiliary voltage generated with lock-in DAC fed into Controller 1
- "off" : Feed path in Controller 1 interrupted

Lock-in aid: (lock-in aid for 220 MHz circuit)

- "on" : 220 MHz control loop interrupted, lock-in aid path in Controller 2 made (feeding of 11 MHz phase meter signal)
- "off" : 220 MHz control loop made

Carrier phase meter: (frequency generator)

- "Internal" : Frequency generator set for internal bit rate
- "External" : Frequency generator synchronized with external clock
- Internal/External switching:
  During the switching operation, a lock-in aid in the carrier phase meter briefly becomes active, ensuring that the frequency generator can synchronize with the external clock.

9.2 CIRCUITRY DESCRIPTIONS

9.2.1 FREQUENCY GENERATOR (A)

9.2.1.1 Carrier oscillator [5/2019-P]

The carrier oscillator is a voltage-controlled oscillator covering the frequency range of approximately 200 to 400 MHz.

Generation of oscillations:

The frequency is determined by the tank circuit comprising capacitance diode Gl 2 and L 6. This is a coaxial, capacitively shortened $\lambda/4$ resonant-line circuit.

In order to obtain the necessary frequency variation, the anode of Gl 2 must be supplied with a negative bias voltage. This bias voltage is supplied via the filter sections R 3/C 5, R 5/C 4 and R 15/C 17.

The control voltage is supplied via a low-pass filter comprising C 35, L 4/C 34, C 7 and L 5 with a peak at approx. 70 kHz.
Together with L 5/C 32 and C 31 in the carrier phase meter, this filter forms the control voltage filter.

The oscillation is generated with a Hartley circuit. T 2 is connected to the tank circuit via coupling capacitors C 14 and C 15 for this purpose. The DC voltage at C 13 determines the amplitude of the oscillation (see below).

Coupling out:

The frequency-determining tank circuit and the crystal circuit are located in a separate housing. The signal voltage is coupled out inductively. The base DC voltage for the first buffer stage (divider R 17, R 18) is generated at the "cold" end of the coupling-out loop. The low-pass filter comprising R 19, C 21 suppresses unwanted resonances.

The first buffer stage (collector stage T 4) decouples buffer amplifier DSS 1 from the coupling-out loop. The signal voltage is split over three branches at the output of the buffer amplifier.

The signal is passed to the carrier phase meter (6) and the mixer (7) via buffer stages DSS 2 and DSS 3, respectively.

The third branch leads to the peak rectifier in the amplitude controller.

Amplitude control:

The peak rectifier consisting of Gl 3, Gl 4 and C 26 supplies a negative DC voltage to one input of the differential amplifier T 5, T 6. The reference voltage variable with P 2 is present at the other input. The direct current of T 2 (and thus the oscillation amplitude) is varied via T 3 until the voltage output by the rectifier and the reference voltage are identical.

Operating voltage filtering:

The positive operating voltage of +9 V is generated with controller IC 1 (noise suppression > 70 dB).
P 1 can be used to set the voltage to the correct value.

The negative operating voltage for amplitude control is freed from interference by T 1/C 5.

In order to prevent blocking of the emitter junction when the operating voltages are switched on, diode Gl 1 is used to limit the voltage at the emitter of T 2 to max. +0.7 V.

9.2.1.2 Carrier phase meter [6/2019-Q]

"Internal" setting: Multiplier-by-ten loop for f_R = crystal-stabilized lock-in osc. freq.
= 22.07 ... 38.7 MHz

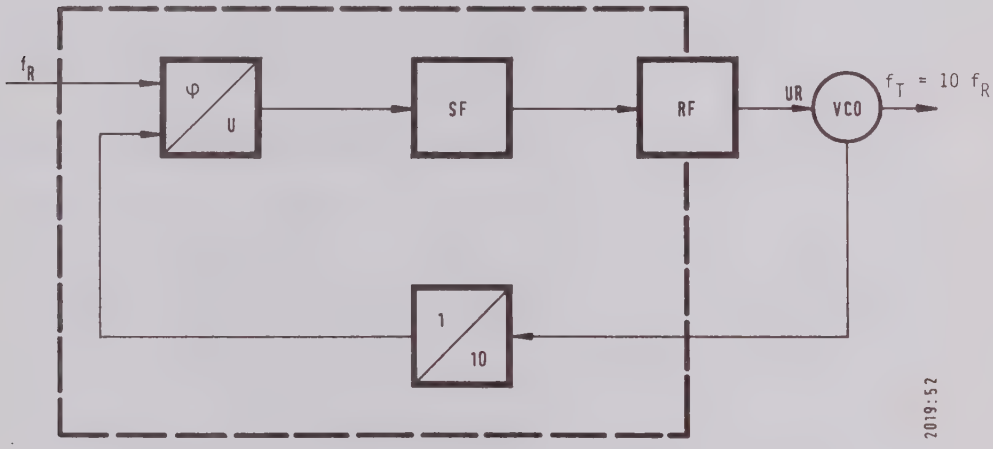


Fig. 9.2-1 "Internal" setting

φ/U = Frequency-sensitive phase meter 12040 -> ∞ Large lock-in range
SF = Loop filter = PI controller; ensures pass frequency of the open circuit f_D = 10 kHz with phase reserve φ_R = 39°
RF = Control voltage filter = Cauer LP with 2 peaks (70 kHz, 109 kHz), designed to suppress phase meter frequency
VCO = Voltage-controlled LC oscillator with f_T = 160 ... 500 MHz

Useful range: f_T = 220 ... 387 MHz with U_R = -1.5 V ...+8 V

"External" setting: Frequency addition of 22 MHz and $\frac{f_{ext}}{10}$ and multiplication by 10

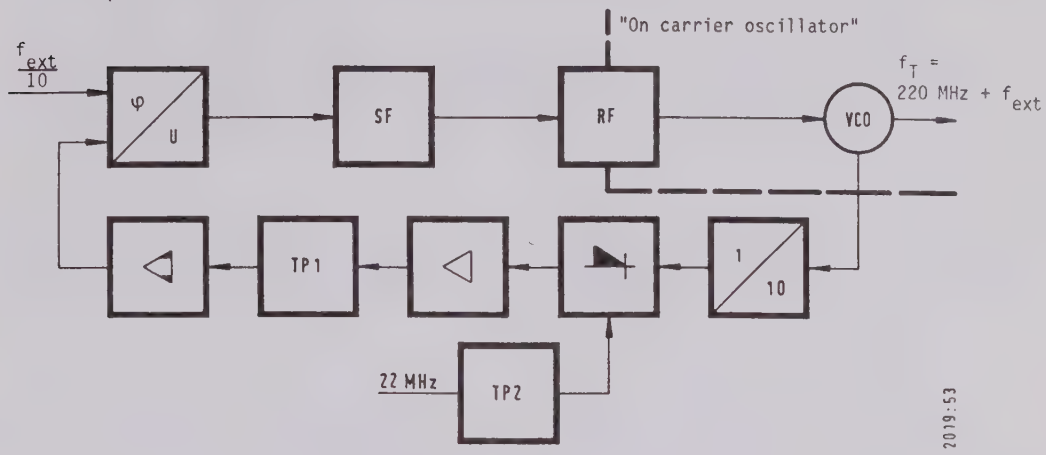


Fig. 9.2-2 "External" setting

LP-2: Attenuates k_2 of 22 MHz: 44 MHz by 11 dB in relation to 22 MHz

Attenuates 22 MHz by 20 dB due to mixer harmonic distortion

▷ : Amplifies signal at mixer output by 26 dB

LP-1: Cauer LP with 3 peaks (incl. 22 MHz), f_{3dB} = 17 MHz

Ripple approx. 3 dB, return loss 63 dB

▷ : Limits sine wave to ECL signal

Switching from "Internal" <-> "External" by relay:

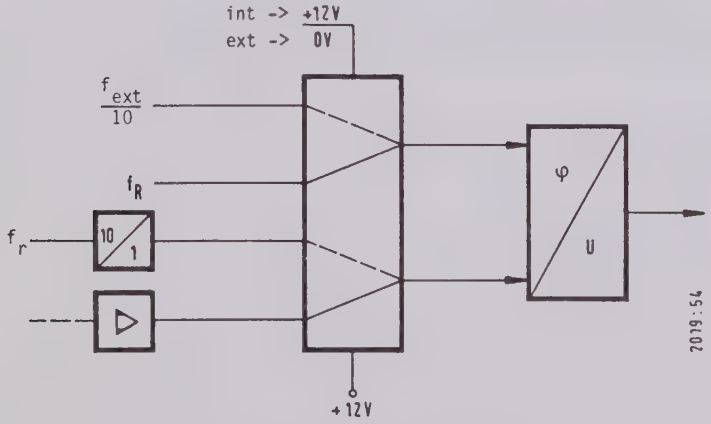


Fig. 9.2-3 "Internal" <-> "External" switching

An offset setting is provided in the loop filter due to the undefined characteristic at the zero point of the phase meter.

Lock-in problems in "External" setting:

For large f_T, TP 1 blocks, Φ/U reports f_T too small } U_R in upper corner

For small f_T, the control direction may be reversed due to the mixer } U_R in lower corner

Both states can be caused by undefined switching sequences and times of the relay.

Lock-in aid: During switching, the feedback path of the OP in the SF is shorted with an FET; this prevents charging of the integrating capacitor and, consequently, drifting of U_R.

9.2.1.3 Lock-in oscillator [6/2019-R]

The lock-in oscillator can generate a maximum of 10 lock-in frequencies and is fitted with up to 10 selectable crystals for this purpose.

The individual crystals are switched on via addresses applied to decoder IC 102.

The crystal is driven via T 102 and T 103. The parallel-resonant circuit comprising U 101 and Gl 104 ... Gl 106 ensures that the crystals oscillate at the third harmonic. The tank circuit is tuned to the individual crystal frequencies via the capacitance diodes.

The tuning voltage of the tank circuit is temperature-compensated by Gl 117.

The secondary winding of transformer U 101 couples out the signal. T 104 forms the buffer stage on the output side.

The amplitude is controlled by peak rectification with Gl 103 and changing the dynamic impedance of Gl 101 and Gl 102. The dynamic output impedances represent a variable load in the feedback path.

The tuning voltages for the tank circuit are also selected via decoder IC 102 and switching transistors T 105 ... T 114.

To prevent the noise and jumping of cermet trimmers P 100 ... P 109 for setting the tuning voltage from generating phase noise in the output frequency due to the high sensitivity, only small trimmer values are suitable, i.e. approx. 5% of the total resistance. The series resistor thus becomes the alignment value and can only be fitted after measuring.

Of the 10 possible frequencies (1 x EXTERNAL, 9 x INTERNAL), 6 frequencies are fitted as standard:

22.0000 MHz	(EXTERNAL)
22.2048 MHz	(Bit rate 2048 kbit/s)
22.8448 MHz	(Bit rate 8448 kbit/s)
24.5776 MHz	(Bit rate 25776 kbit/s)
25.4368 MHz	(Bit rate 34368 kbit/s)
35.9264 MHz	(Bit rate 139264 kbit/s)

The other 4 frequencies can be fitted as per customer requirements.

9.2.1.4 Clock divider [6/2019-S]

When set to "EXTERNAL", the clock divider receives an external clock, divides its frequency by 10 and passes this signal to the carrier phase meter (ECL signal) and hit counter (TTL signal). The input is AC-coupled and its resistance is 75 Ω.
It is protected against overvoltage up to ± 15 V.
A square-wave signal is required as input signal (e.g. ECL signal) to ensure reliable functioning, since the edge steepness of a sinusoidal signal is inadequate, particularly at low frequencies. An MC 10H116 is used as line receiver.

9.2.2 INPUT CIRCUIT (B) [2/2019-V]

The input circuit processes digital signals with bit rates of 600 kbit/s to 168 Mbit/s and logic levels of 50 mVp to 4 Vp, passing them to the sawtooth phase meter (7) and the code error circuit (3).

9.2.2.1 Signal path

The input signal passes from Bu 1 on the front panel via the dividers to the equalizer amplifier. The 3 dB divider is used to improve the input return loss. The 10 dB and 20 dB dividers are controlled as a function of level or, if the equalizer is operating, switched in accordance with the bit rate and code.

The reference potential of the 75 Ω input resistor can be switched between 0 V and -2 V (for NRZ/ECL and RZ/ECL). The input of the equalizer amplifier is provided with an overvoltage protection circuit comprising the diodes Gl 1, Gl 2 and Gl 15.

The equalizer amplifier T 2 ... T 8 has a gain of approx. 14 dB in normal mode (flat).

Buffer stages T 9 ... T 11 distribute the data signal to the "Equalized data signal" output socket [32], to the twin comparator IC 11 and to the peak rectifier and zero-point controller IC 3, IC 4. Only comparator IC 11/1 operates for binary data signals. The data signal passes via the EXOR gate IC 14/1 to the sawtooth phase meter (7) and via IC 14/2 to the code error circuit (3). IC 14/1 can be used to invert the data signal for the sawtooth phase meter. In the case of ternary data signals, the positive pulses are sampled with IC 11/1 and the negative pulses with IC 11/2. For the sawtooth phase meter, both data streams are combined via a WIRED-OR for clock recovery and phase jitter evaluation. The DA^+ and DA^- data streams are fed to code error circuit (3) separately.

9.2.2.2 Peak rectifier

The signal present at the peak rectifier is the same as that at evaluation comparators IC 11. For RZ and NRZ, as well as for ternary signals, the decision thresholds for the evaluation comparators IC 11 are derived from the peak value. Similarly, the peak value is also used as a control criterion for equalizer control.

Mode of operation: IC 3/1 provides output pulses, which are integrated with IC 4/1, until the output voltage of IC 4/3 (= threshold for comparator IC 3/1) is equal to the peak value of the signal applied.

The peak value at IC 4/Pt. 14 is passed to comparators IC 10, which are used for level monitoring. Together with the setting of the 10 dB and 20 dB dividers, the information from the comparator is used to derive the instrument messages "INPUT SIGNAL TOO LOW" (IC 10/2 = H and no divider switched) or "INPUT OVERLOAD" (IC 10/1 = H and both dividers switched).

9.2.2.3 Zero-point control

Zero-point control is used to recover the DC voltage with codes affected by a DC component (RZ and NRZ).

A DC voltage is superimposed on the output signal at buffer stages T 9 ... T 11. Its amplitude is varied until comparator IC 3/2 ceases to supply output pulses. As the reference input of the comparator is connected to earth, this ensures that the minimum signal level at the comparator input is shifted to 0 V. The output pulses of comparator IC 3/2, integrated with IC 4/3, form the offset voltage which, in the case of the RZ and NRZ modes, is passed to the buffer stages via switch IC 5 and power amplifier IC 2/1, T 13, T 14.

9.2.2.4 Threshold switching

IC 13 switches the thresholds for the evaluation comparators IC 11 in accordance with the code. In the case of binary signals without DC component (e.g. CMI) and with clock signals, the decision threshold of IC 11/1 is set to 0 V. For binary signals with DC component, the threshold is set to 50% of the peak value. For binary signals, the threshold of comparator IC 11/2 is set to -2 V, meaning that the negated output (Pt. 15) remains at "L" level, regardless of the input signal.

For ternary data signals, the decision threshold of evaluation comparator IC 11/1 is set to 50% of the peak value, with the result that the DA^+ data stream appears at its output. The decision threshold of evaluation comparator IC 11/2 is set to -50% of the peak value; the DA^- data stream appears at one output.

9.2.2.5 Equalizer mode ($\sqrt{f}$)

In $\sqrt{f}$ mode, the equalizer amplifier is designed to compensate for the frequency-dependent loss caused by a longer cable between signal source and PJM-4. It is assumed in this context that the data signal at the signal source has a certain nominal level. The negative peak value of the nominal level, corrected by the gain of the equalizer amplifier (in "flat" mode), including dividers, is fed in at the summation point of integrator IC 4/4. The integrator changes the control voltage for the PIN diodes in the equalizer amplifier until the peak value of the data signal at the output of the equalizer amplifier is equal to the reference. The gain of transistor stages T 3 to T 8 is increased via the PIN diodes with RC sections as a function of the frequency. The maximum change in gain is 12 dB at f = 70 MHz.

9.2.3 CODE ERROR (C)

9.2.3.1 Code error 1 [3/2019-AL]

The Code error 1 card determines the code errors in the received data signal and counts them. This circuit can examine the following codes for code errors:

a) CMI
b) AMI
c) HDB3

At the same time, a check is also made whether an AIS signal (Alarm Indication System) is transmitted (block circuit diagram 9.2-4).

9.2.3.1.1 "Delay correction" function block

Since it is essential for the function of the Code error 1 card that the clock lags 90° behind the data, instrument-specific delay variations and transmission rate-dependent delay (phase) changes must be equalized. Furthermore, the basic delay in the clock path is greater than that in the two data paths. In order to restore the correct temporal relationship between the two types of signal, the two data signals are delayed 10 ns by cable, while the necessary alignment in the clock path is performed by means of the "delay correction" circuit. This circuit is of SMD design and is soldered onto the Code error 1 card.

The sinusoidal clock present at the input is amplified by a two-stage, negative feedback amplifier (3 T 11, 3 T 12). The feedback element of the voltage feedback consists of two series-connected capacitance diodes (3 Gl 11, 3 Gl 12) parallel to a resistor (3 R 9). The capacity of the diodes can be varied with a DC voltage applied externally (U_V; Pin 10); the phase caused by this amplifier is also varied in this way. 3 R 12 matches the amplifier output ($R_i \approx 0$) to the downstream six-stage delay line, which is adjustable in steps ($\Delta\tau \approx +0.45$ ns per step).

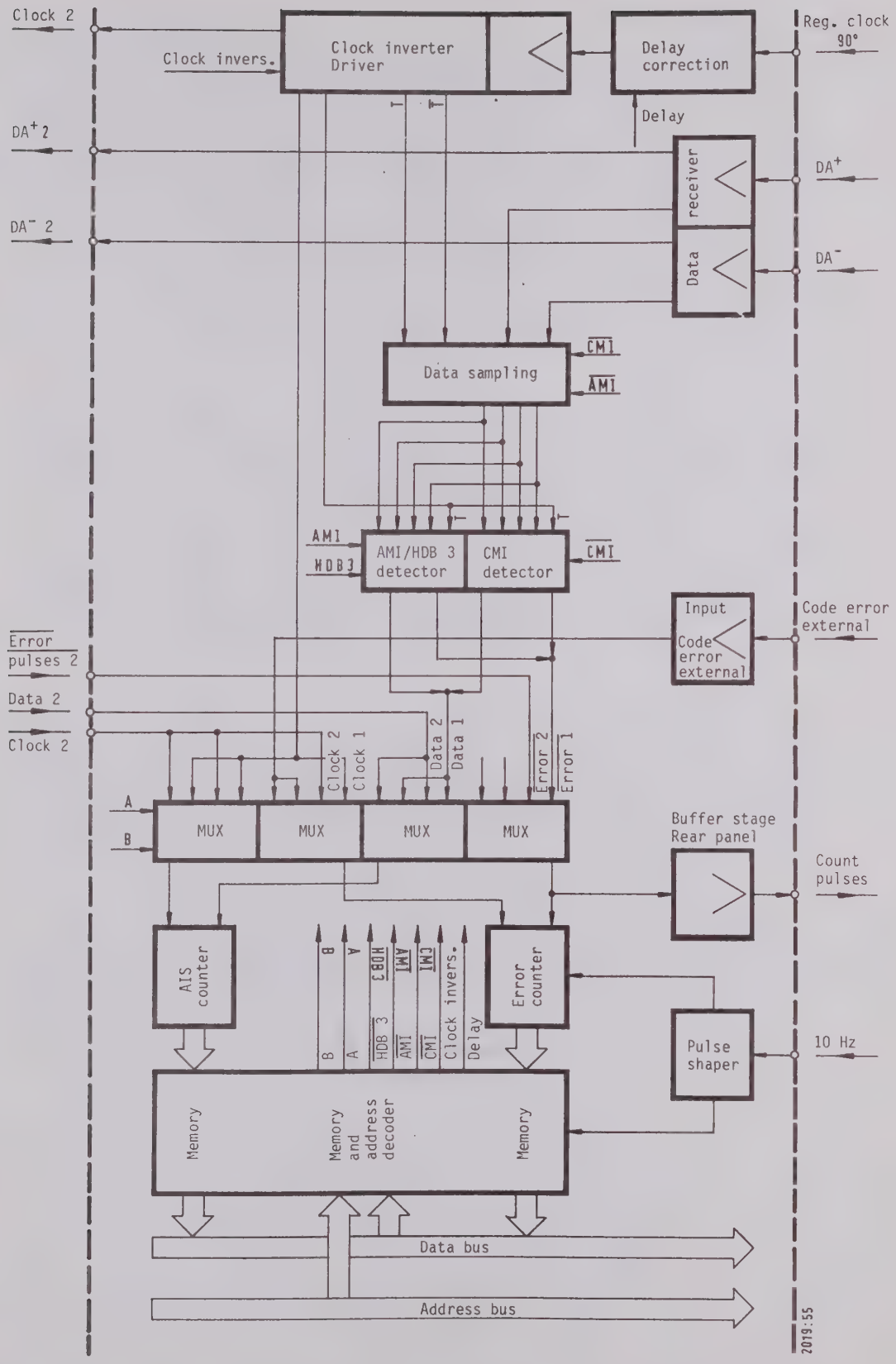


Fig. 9.2-4 Code error 1

9.2.3.1.2 "Clock inverter/Driver" function block

In this block, the sinusoidal clock is converted into a square-wave signal and a suitable alignment performed to eliminate any possible asymmetry of the square-wave signal.

Since the phase between the two data signals (Da^+, Da^-) and the regenerated 90° clock can be +90° or -90°, depending on the operating status of the instrument ("NORM", "INVERT"), an inverter (3 IC 3), controlled with the "Clock invers." signal, is used to restore the correct phase position. In order to prevent a reduction of the edge steepness of the clock signal due to excessive fan-in, all gates of 3 IC 3 are operated in parallel as clock drivers.

The clock signal conditioned in this way is used as a clock signal for Code error 1 and, at the same time, after decoupling via 3 IC 1, passed to Code error 2 (4) (option) via connector 3 11.

9.2.3.1.3 "Data receiver" function block

In order to prevent reflections on the two data lines Da^+ and Da^-, the lines are fed from sources with $R_i = Z_o = 75\ \Omega$ (2 IC 14/2; 2 R 158; 2 C 73; 2 IC 14/3; 2 R 159; 2 C 74) and terminated with $R_{ab} = Z_o = 75\ \Omega$ to earth at the end, i.e. "H" = -0.4 V and "L" = -0.8 V. However, since signals with ECL level are required, line receivers are connected downstream (3 IC 1), the input reference voltage of which is variable in order to align the symmetry of data signals. The other line receivers available in 3 IC 1 are used to pass the decoupled signals Da^+2, Reg. clock 2 and Da^-2 to Code error 2 (3 10,11,12).

9.2.3.1.4 "Data sampler" function block

To detect the exact signal status, the two data streams Da^+ and Da^- are sampled by D-FFs (3 IC 4), depending on the code set on the instrument.

a) AMI, HDB3
   Both the Da^+ signal and the Da^- signal are sampled at time T/4 of a bit period.
   Fig. 9.2-5 and Fig. 9.2-13 or Fig. 9.2-14

b) CMI
   The Da^+ signal is sampled at time T/4 and at time 3T/4.
   Fig. 9.2-5 and Fig. 9.2-8

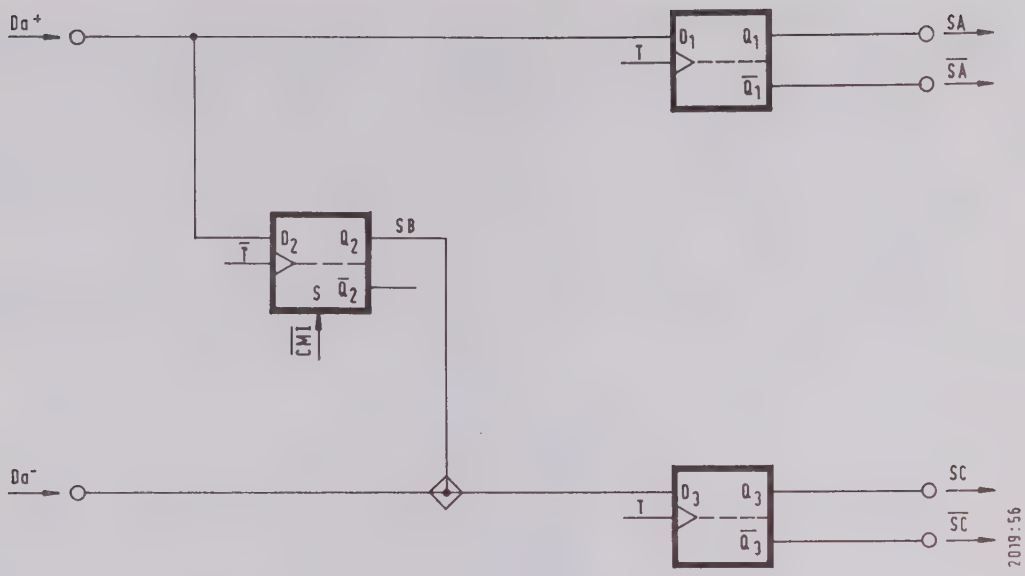


Fig. 9.2-5 Sampling circuit

9.2.3.1.5 "CMI detector" function block

This circuitry section has the task of detecting code errors in the CMI (Code Mark Inversion) code. CMI is a binary line code where an NRZ signal is coded in accordance with the following rules:

	NRZ signal	CMI signal	CMI sampled at T/4	CMI sampled at 3T/4
Clock period				
Logic Zero	"H" "L"	"H" "L"	"H" "L"	"H" "L"
Logic One	"H" "L"	"H" "L" or "H" "L"	"H" "L"	"H" "L"

Fig. 9.2-6 CMI coding and sampling

The polarity of the "1" bits must alternate in the CMI code. A violation of this rule is rated as a CMI code error.

The circuitry of the CMI detector and the associated timing diagram can be found in Fig. 9.2-7 and Fig. 9.2-8.

Since the data sampling principle causes a temporal offset of one clock period between the signals sampled at T/4 and 3T/4, synchrony is restored by a D-flip-flop (3 IC 6/1). An NOR gate then forms the NRZ signal (evaluation of the "Q" combination). To evaluate the code errors, the polarity of the last "1" bit is stored in a flip-flop (3 IC 6/2) and compared with the polarity of the following "1" bit (Fig. 9.2-8), i.e. the circuit supplies a pulse with the length of one clock period for each code error.

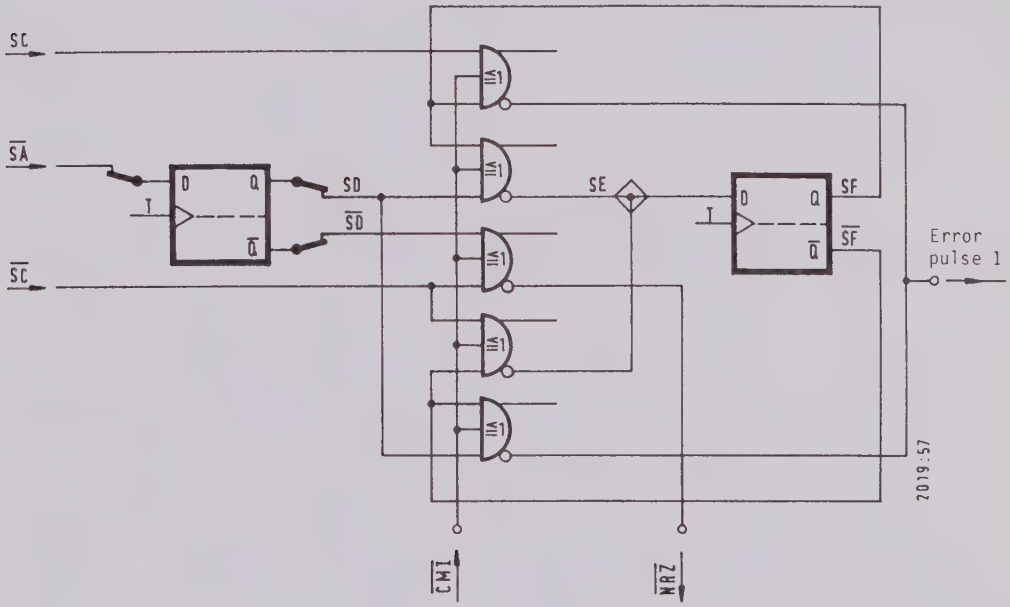


Fig. 9.2-7 CMI code error detector

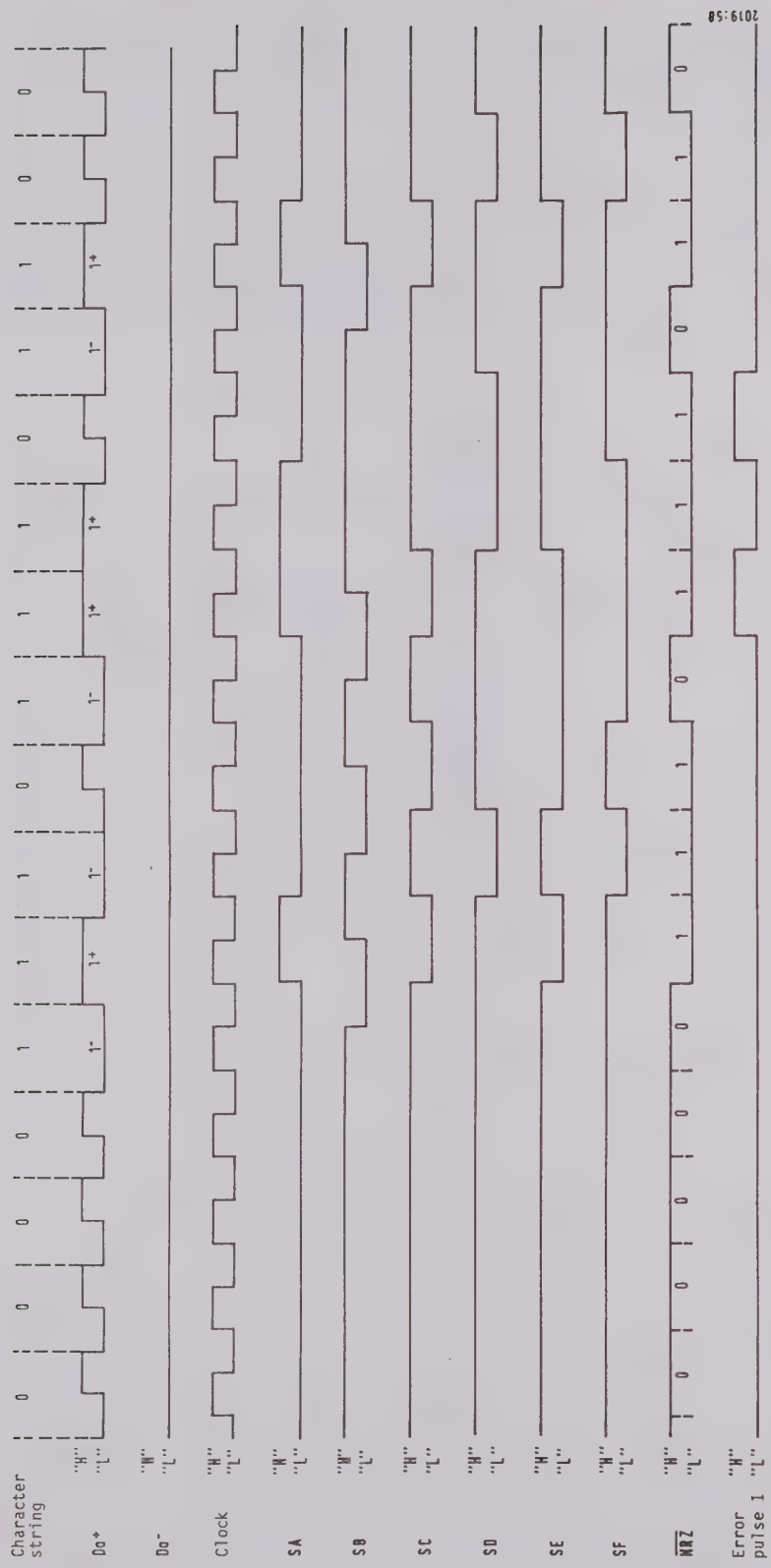


Fig. 9.2-8 Timing diagram of the data sampler and error detector for CMI

9.2.3.1.6 "AMI/HDB-3 detector" function block

AMI detector

The AMI line code (Alternate Mark Inversion) is a ternary code, i.e. there are three different logic levels. The line signal is formed according to the following rules:

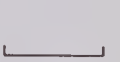
	NRZ signal	AMI signal	Da^+ sampling	Da^--sampling
Clock period				
Logic Zero	"H" "L"	"H" "L"	"H" "L"	"H" "L"
Logic One	"H" "L"	"H" "L" "H" or "H" "L" "H"	"H" "L" "H" "L"	"H" "L"  "H" "L"

Fig. 9.2-9 AMI/HDB-3 coding and sampling

The polarity of the "1" bits must alternate in the AMI code. A violation of this rule is rated as an AMI code error.

The circuitry of the AMI detector and the associated timing diagram can be found in Fig. 9.2-7 and Fig. 9.2-13.

The $\overline{NRZ}$ signal is formed by combination of the sampled signals Da^+ and Da^- in an OR circuit (3 IC 5/1) and subsequent inversion with a NOR gate (3 IC 5/2).

The polarity of the last "1" bit is stored in J-K flip-flop (3 IC 10/1) and then compared with the polarity of the following "1" bit (3 IC 11/1, 3 IC 11/2). An error pulse occurs at the output of 3 IC 12/2 or 3 IC 12/3 if two consecutive "1" bits with the same polarity are detected.

HDB-3 detector

The HDB-3 line code differs from the AMI code only in the coding of zero sequences where the number of zeros is 4 or more. The differences in relation to AMI are compiled in the following table:

	AMI zero sequence	HDB-3 zero sequence	Code rule
Clock			
Line signal	"H" "L" "H"	"H" "L" "H"	If the last violation bit was negative and the last "1" or additional bit was positive
		"H" "L" "H"	If the last violation bit was negative and the last "1" or additional bit was negative
		"H" "L" "H"	If the last violation bit was positive and the last "1" or additional bit was negative
		"H" "L" "H"	If the last violation bit was positive and the last "1" or additional bit was positive

V = Violation bit
Z = Additional bit

Fig. 9.2-10 HDB-3 coding

The code rules mean that the violation bits must alternate. If this rule is violated, this is rated as a code error.

As with the AMI detector, the polarity of the last "1" bit is stored in a J-K flip-flop (3 IC 10/1) and compared with the polarity of the subsequent "1" bit (3 IC 11/1, 3 IC 11/2). If the polarity has not changed, this is rated as a violation bit and its polarity is stored in another J-K flip-flop. If another violation bit occurs, the polarity is compared and, if it is the same, an error pulse output.

The $\overline{NRZ}$ signal is formed as for AMI; the error made during this process (violation bits are rated as "1" bits) has no effect, since this information is only used for AIS detection.

Although the monitoring of zero sequences is not used as an error criterion according to CCITT O.161, the circuit evaluates them with the D-FFs 3 IC 6/5, 3 IC 6/6, 3 IC 9/1, 3 IC 9/2 and gate 3 IC 12/1. The evaluation mode is freely selectable with bridges 3 Br C, Br D, Br A, Br C in accordance with the following table:

Br C-D	Br A-B		
-o o-	-o o- -o-o-	0 0 0 0 No HDB-3 code error	
-o-o-	-o o-	0 0 0 0 as HDB-3 Code error	Code error = Number of zeros - 3
-o-o-	-o-o-	0 0 0 0 as HDB-3 Code error	Code error = INT (Number of zeros / 4)

Number of zeros

Fig. 9.2-11 Selectable error criteria

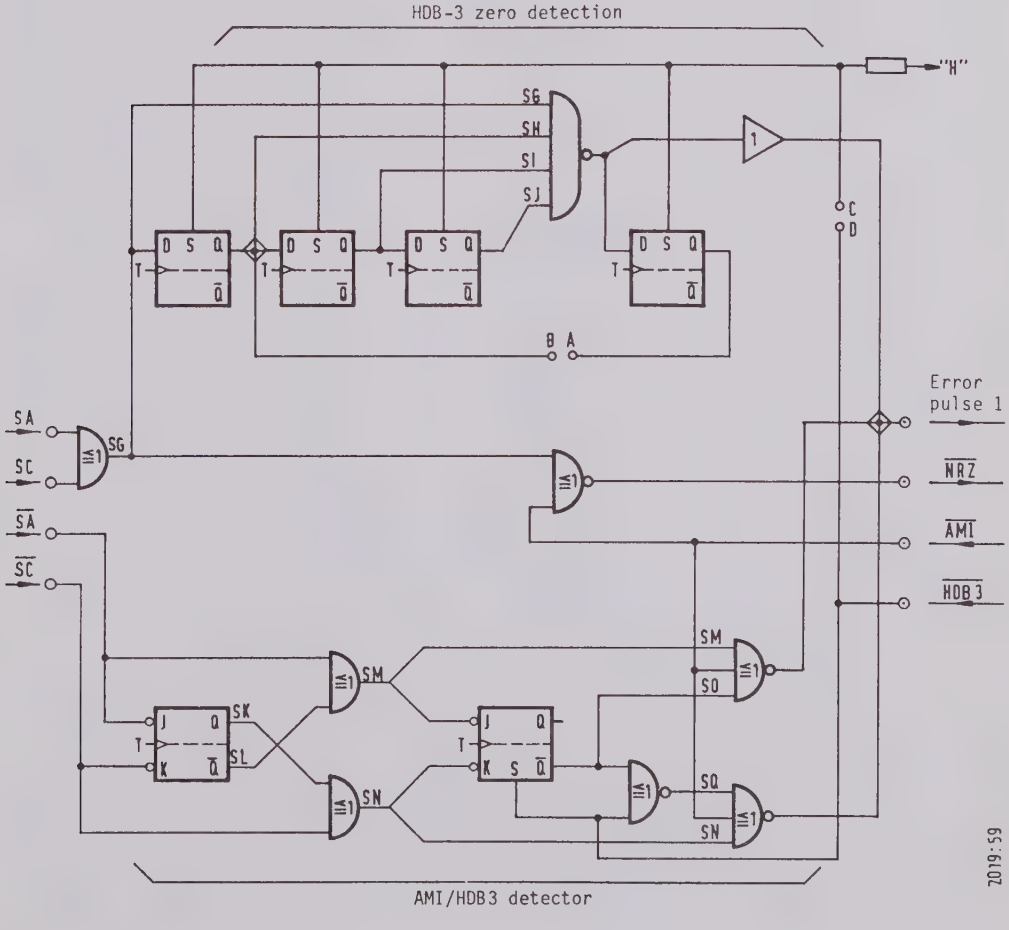


Fig. 9.2-12 AMI/HDB-3 detector

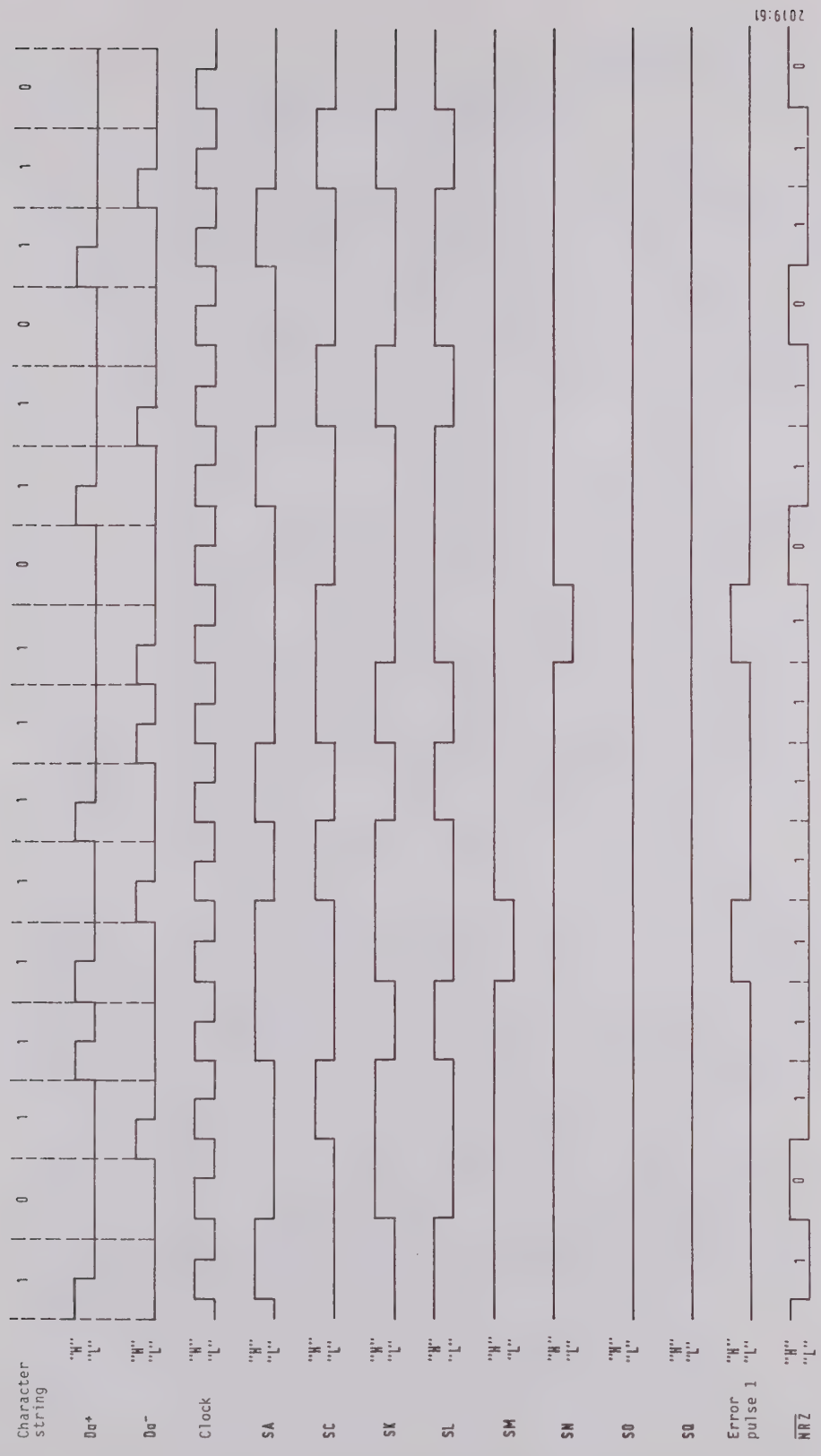


Fig. 9.2-13 Timing diagram of the data sampler and error detector for AMI

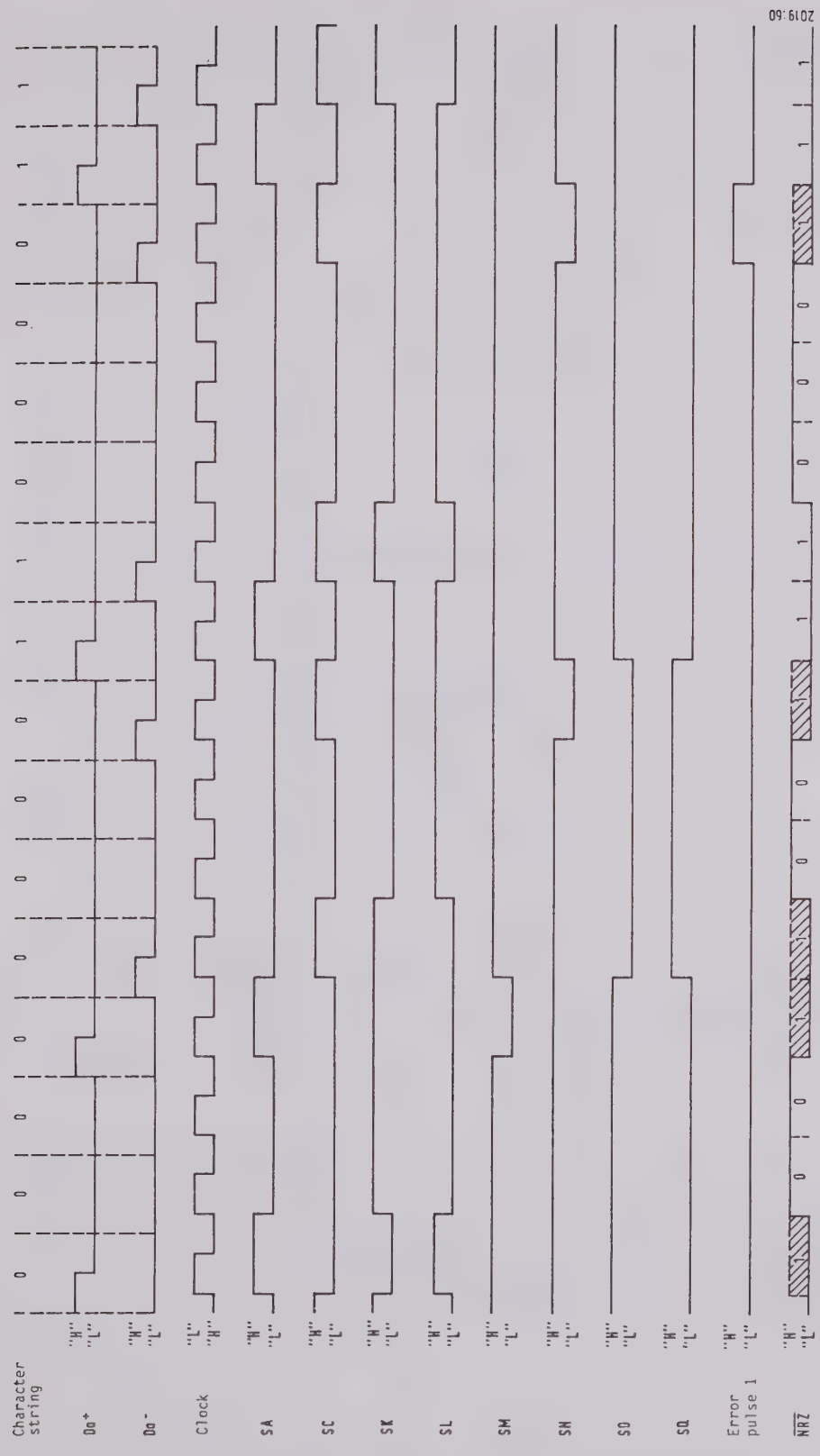


Fig. 9.2-14 Timing diagram of the data sampler and error detector for HDB-3

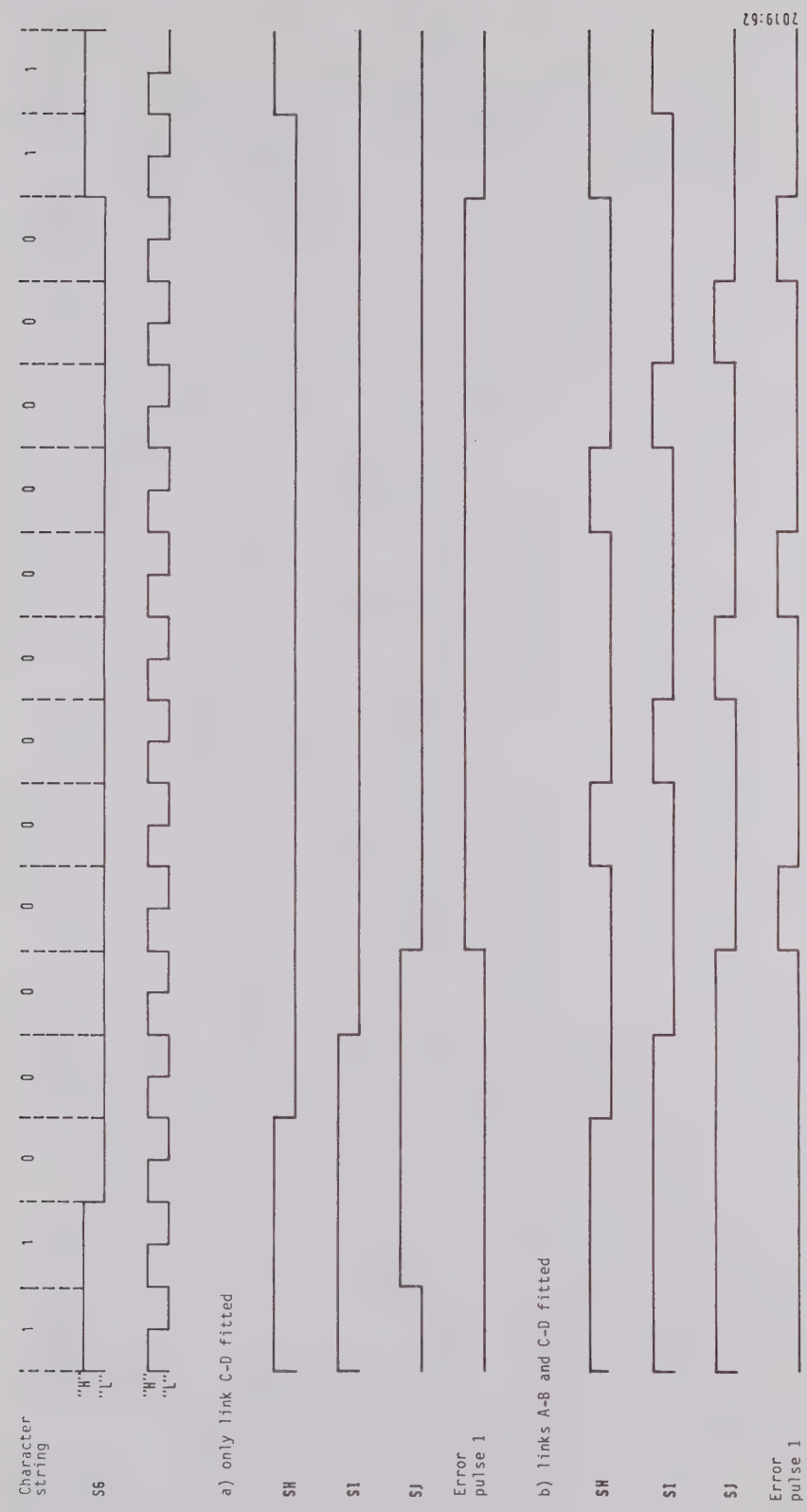


Fig. 9.2-15 Timing diagram of the HDB-3 zero detector

9.2.3.1.7 "External code error input" function block

The "Exernal code error" input is provided to allow acquisition of the results of existing external error detectors.

The type of input signal required can be selected by means of a switch and is then converted to ECL level.

Switch setting	L	H	Input impedance
I ≙ TTL	0 V <-> 0.8 V	2.4 V <-> 5 V	10 kΩ
II	0 V <-> 0.3 V	1 V <-> 5 V	10 kΩ
III ≙ ECL	-1.8 V <-> -1.6 V	-1 V <-> -0.8 V	75 Ω

Fig. 9.2-16 Input sensitivity as a function of switch setting

A transition from "L" to "H" is rated as an error.

9.2.3.1.8 "Multiplexer" function block

In order to operate the error counter and/or AIS counter from different signal sources, a multiplexer is necessary, with which the signal sources can be selected in accordance with the following scheme:

Control word		AIS	Code error
B	A	signal source	signal source
L	L	Code error 1	Code error 1
L	H	Code error 2	Code error 2
H	L	Code error 1	External
H	H	Code error 2	External

Fig. 9.2-17 Multiplexer truth table

9.2.3.1.9 "Rear panel buffer stage" function block

To allow external evaluation of the error pulses, these are adjusted to a pulse width of 0.5 bit by combination with the clock in a NOR circuit (3 IC 14/1) and passed to the "COUNT PULSES" output.

9.2.3.1.10 "Error counter" function block

The error counter has the task of counting the incoming error pulses and making the result available to the processor.

Since the frequency of the input signal can be up to 167.1 MHz, due to the mode of operation of the error detectors, a high-speed ECL 16:1 divider (3 IC 25) is provided as the first stage. The divided signal is then set to HC level and further processed in a gate array (3 IC 26) (contains counters and necessary peripherals).

9.2.3.2.3 "Error detector" function block

4B3T code

The designation 4B3T code is used as a general term for various codes, all of which have one common feature: 4 binary input bits are translated into 3 ternary output bits. Depending on code, 2, 3 or 4 alphabets are used for translation.

4B word	3T word and following status (FS)								
	Status S 1	FS	Status S 2	FS	Status S 3	FS	Status S 4	FS	
0000	+ 0 +	3	0 - 0	1	0 - 0	2	0 - 0	3	
0001	0 - +	1	0 - +	2	0 - +	3	0 - +	4	
0010	+ - 0	1	+ - 0	2	+ - 0	3	+ - 0	4	
0011	0 0 +	2	0 0 +	3	0 0 +	4	- - 0	2	
0100	- + 0	1	- + 0	2	- + 0	3	- + 0	4	
0101	0 + +	3	- 0 0	1	- 0 0	2	- 0 0	3	
0110	- + +	2	- + +	3	- - +	2	- - +	3	
0111	- 0 +	1	- 0 +	2	- 0 +	3	- 0 +	4	
1000	+ 0 0	2	+ 0 0	3	+ 0 0	4	0 - -	2	
1001	+ - +	2	+ - +	3	+ - +	4	- - -	1	
1010	+ + -	2	+ + -	3	+ - -	2	+ - -	3	
1011	0 + -	1	0 + -	2	0 + -	3	0 + -	4	
1100	+ + +	4	- + -	1	- + -	2	- + -	3	
1101	0 + 0	2	0 + 0	3	0 + 0	4	- 0 -	2	
1110	0 + -	1	0 + -	2	0 + -	3	0 + -	4	
1111	+ + 0	3	0 0 -	1	0 0 -	2	0 0 -	3	
0000	0 0 0	1	0 0 0	2	0 0 0	3	0 0 0	4	*

* Assignment applies for the decoder only

Fig. 9.2-19 Code table, MMS 43 (BP) code
(Modified Monitored Sum 4B 3T Code)

By way of example, Fig. 9.2-19 shows the code alphabets of a 4B3T code used by the German Bundespost and Fig. 9.2-20 the result of coding a non-scrambled continuous "1" sequence.

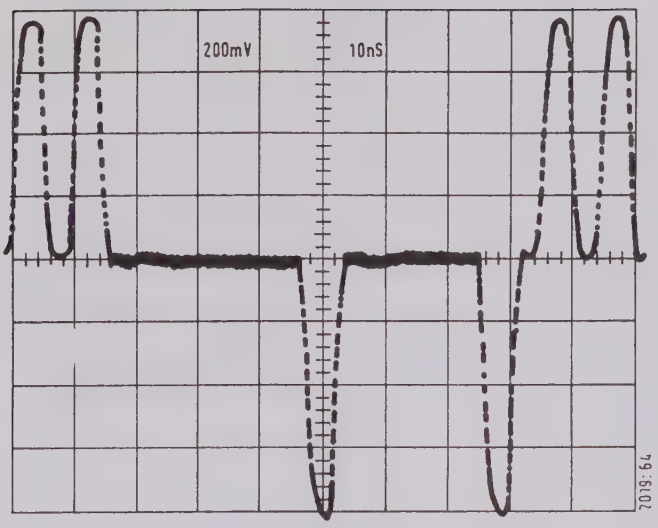


Fig. 9.2-20 Non-scrambled continuous "1" sequence in 4B3T code (MMS 43)

For evaluating code errors in 4B3T codes, the Code error 2 card uses the Running Digital Sum (RDS) method, i.e. the incoming bits are continuously added in accordance with their value (0, +1, -1) and checked to establish whether the result is within the code-specific range of values (Fig. 9.2-21).

Send signal word	n	n+1	n+2	n+3	n+4	n+5	n+6	n+7	n+8	n+9
B word	1111	1101	1111	0011	1101	0111	0000	1101	1101	0011
3T word	++0	0+0	00-	00+	-0-	-0+	0-0	0+0	0+0	00+
Receive signal error-free 3T word	++0	0+0	00-	00+	-0-	-0+	0-0	0+0	0+0	00+
RDS[1)]	+2+3+3	+3+4+4	+4+4+3	+3+3+4	+3+3+2	+1+1+2	+2+1+1	+1+2+2	+2+3+3	+3+3+4
Receive signal with errors 3T word	++$\underline{+}$	0+0	00$\underline{+}$	00+	-0-	-0+	0-0	0+0		
RDS[1)]	+2+3+4	+4+5+5	(+6) +5+5+5	(+6) +5+5+5	+4+4+3	+2+2+3	+3+2+2	+2+3+3		
Error pulse	-	-	1.	2.	-	-	-	-		
4B word	11$\underline{00}$	1101	$\underline{00}$11	0011	1101	0111	0000	1101		

1) RDS of word n-1 set to +1

$\underline{+}$ = Transmission error

$\underline{00}$ = Sequence error

Fig. 9.2-21 Example of B3T coding and error evaluation

The value range implemented in the circuitry:

$0 \cong RDS \cong 5$

allows code error evaluation for the following 4B3T codes:

- MMS-43-BP (DBP; 4 alphabets)
- MMS-43 (Telettra; 4 alphabets)
- MS-43 (GEC/Plessey; 3 alphabets)
- Fomot (Philips/Tekade; 4 alphabets).

5B6B code

In this code, 5-bit binary blocks are converted into 6-bit binary blocks (= NRZ) (Fig. 9.2-22).

5B word		6B word					
		Mode +		Following mode		Mode -	Following mode
0	00000	50	110010	+	50	110010	-
1	00001	51	110011	-	33	110010	+
2	00010	54	110110	-	34	100010	+
3	00011	35	100011	+	35	100011	-
4	00100	53	110101	-	36	100100	+
5	00101	37	100101	+	37	100101	-
6	00110	38	100110	+	38	100110	-
7	00111	39	100111	-	7	000111	-
8	01000	43	101011	-	40	101000	+
9	01001	41	101001	+	41	101001	-
10	01010	42	101010	+	42	101010	-
11	01011	11	001011	+	11	001011	-
12	01100	44	101100	+	44	101100	-
13	01101	45	101101	-	5	000101	+
14	01110	46	101110	-	6	000110	+
15	01111	14	001110	+	14	001110	-
16	10000	49	110001	+	49	110001	-
17	10001	57	111001	-	17	010001	+
18	10010	58	111010	-	18	010010	+
19	10011	19	010011	+	19	010011	-
20	10100	52	110100	+	52	110100	-
21	10101	21	010101	+	21	010101	-
22	10110	22	010110	+	22	010110	-
23	10111	23	010111	-	20	010100	+
24	11000	56	111000	+	24	011000	+
25	11001	25	011001	+	25	011001	-
26	11010	26	011010	+	26	011010	-
27	11011	27	011011	+	10	001010	+
28	11100	28	011100	+	28	011100	-
29	11101	29	011101	-	9	001001	+
30	11110	30	011110	-	12	001100	+
31	11111	13	001101	+	13	001101	-
	ABCDE		ABCDEF			ABCDEF	

Fig. 9.2-22 5B6B code table

For this code, too, the Code error 2 card uses the Running Digital Sum (RDS) method, by which the incoming bits are added consecutively in accordance with the following values:

1 ≙ +1
0 ≙ -1

Send signal Word	n-1	n	n+1	n+2
5B word	XXXXX	01010	01111	00000
6B word	YYYYYY	1 0 1 0 1 0	0 0 1 1 1 0	1 1 0 0 1 0
Receive signal error-free 6B word	YYYYYY	1 0 1 0 1 0	0 0 1 1 1 0	1 1 0 0 1 0
RDS[1)]	+1	+2+1+2+1+2+1	0-1±0+1+2+1	+2+3+2+1+2+1
Receive signal with errors 6B word	YYYYYY	1 0 1 0 1 0	0 1 1 1 1 0	1 1 0 0 1 0
RDS[1)]	+1	+2+1+2+1+2+1	(+4) ±0+1+2+3+3+2	(+4) +3+3+2+1+2+1
Error pulse	-	-	1. = F1	2. = F2
5B word	XXXXX	0 1 0 1 0	1 1 1 1 0	0 0 0 0 0

1) RDS of word n-1 set to +1
[1] = Transmission error
1/0 = Sequence error (error multiplication)

Fig. 9.2-23 RDS and error pulse formation

For an error-free code, the value range is then as follows:

$-3 \leq RDS \leq +3$

Error detector

Code error detection for 4B3T and 5B6B can be achieved with a single circuit, since the same evaluation principle is used for both types of code.

The fundamental mode of operation of the circuit is shown in the diagrams.

The circuit design is inherently self-synchronizing, i.e. the circuit is in synchrony after a maximum of 5 (6) errors or 5 (6) extreme values of the RDS. Since line signals are scrambled, it is ensured that RDS extreme values occur. This is not true for short, non-scrambled bit sequences, and synchronization can only be achieved by means of any error occurring.

The necessary switching of the shift register and the driver circuit in accordance with the selected code is achieved with the switching signal "4B3T".

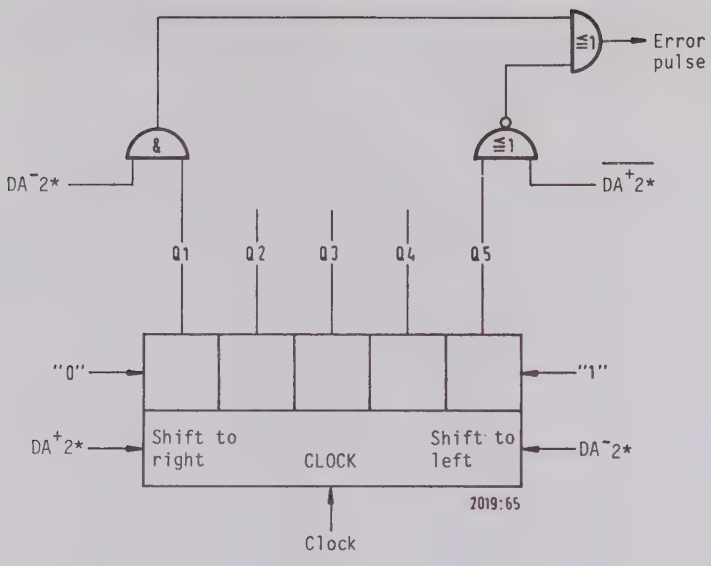


Fig. 9.2-24 4B3T code error evaluation

RDS	$Da^{+}2^{*}$	$Da^{-}2^{*}$	Q_1	Q_2	Q_3	Q_4	Q_5	Error pulses
-1	1	0	0	0	0	0	0	1
0	0	d	0	0	0	0	0	0
1	d	d	0	0	0	0	1	0
2	d	d	0	0	0	1	1	0
3	d	d	0	0	1	1	1	0
4	d	d	0	1	1	1	1	0
5	d	0	1	1	1	1	1	0
5	0	1	1	1	1	1	1	1

Fig. 9.2-25 Operating table

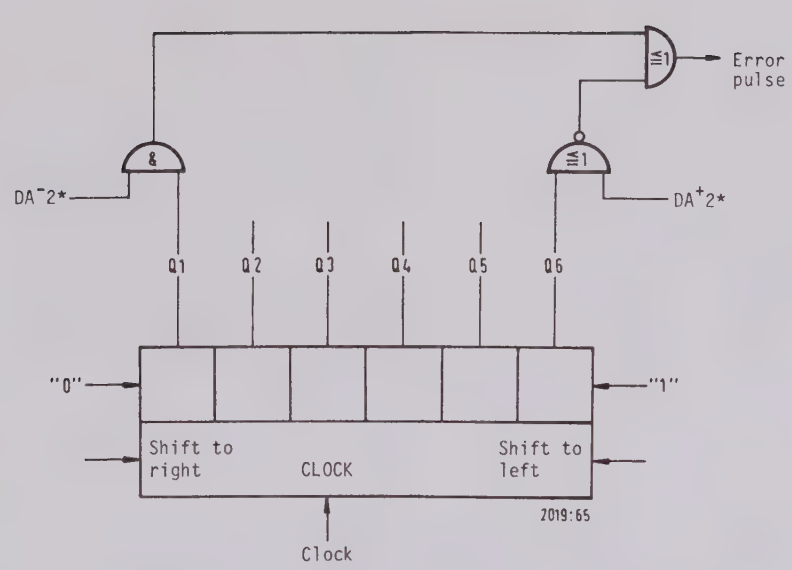


Fig. 9.2-26 5B6B code error evaluation

RDS	$Da^{+}2^{*}$	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Error pulses
-4	0	0	0	0	0	0	0	1
-3	1	0	0	0	0	0	0	0
-2	d	0	0	0	0	0	1	0
-1	d	0	0	0	0	1	1	0
0	d	0	0	0	1	1	1	0
1	d	0	0	1	1	1	1	0
2	d	0	1	1	1	1	1	0
3	0	1	1	1	1	1	1	0
4	1	1	1	1	1	1	1	1

Fig. 9.2-27 Operating table

"Signal driver" function block

Buffer gates in the signal connecting lines between Code error 2 and Code error 1 reduce signal deformation due to reflections at the plug-in connectors. Since AIS detection has not been included, due to the excessive effort (descrambling, decoding), this signal line is connected to logic "0" in order to prevent uncontrolled lighting-up of the AIS lamp.

9.2.4 220 MHz CIRCUIT (D)

9.2.4.1 220 MHz VCO [7/2019-M]

The 220 MHz VCO is an LC oscillator of push-pull design. The tank circuit coil consists of two rigid-sheath coaxial cables L 4, L 5. The tank circuit capacitance is made up of capacitance diodes Gl 1, Gl 2, trimmer capacitor C 19 and capacitors C 9, C 11, C 12 and C 13.

To reduce the steepness of the oscillator, capacitance diodes Gl 1 and Gl 2 are sheared by capacitor C 12. The tuning of the capacitance diodes is based on the point between the cable sections, which is "cold" in high-frequency terms. The DC voltage at this point is generated by voltage controller IC 1. This results in stability and low interference. Coils L 1 and L 2 are used to decouple control voltage 2 from the tank circuit.

The oscillation amplitude of the oscillator is set with trimmer resistor R 1 in the emitter branch.

The two buffer stages T 1, T 2 and T 5, T 6 tap the signal voltage with high impedance at the tank circuit in order to minimize the load on the tank circuit. Each buffer stage consists of two transistors to ensure the greatest possible degree of decoupling. Capacitors C 5, C 22, C 7, C 17 and C 20 are blocking capacitors. The attenuator beads L 3, L 6 and the T-section R 28, C 23, R 24 limit the bandwidth and prevent spurious RF oscillations.

9.2.4.2 Controller 2 [7/2019-N]

Several functions are implemented in Controller 2 (also see Section 9.1.3.1).

In "normal" mode : PI controller for 220 MHz circuit
Lock-in detection and monitoring for 11 MHz circuit

In "lock-in aid" mode : PI controller for "auxiliary" PLL

In "normal" mode, the PI controller is fed with the output signal $U_{\varphi 2}$ of the sawtooth phase meter. The low-frequency signal components are fed via the I path (DC coupling) and the higher-frequency components via the P path (AC coupling).

The adjustable divider in the P path is used to set the gain and, thus, the control limit frequency of the 220 MHz PLL circuit.

In "lock-in aid" mode, the PI controller receives its input signal from a lock-in aid circuit, which conditions the output signal $U_{\varphi 1}$ of the 11 MHz phase meter accordingly.

The lock-in aid circuit also supplies the lock-in detection circuit which checks the lock-in status of the 11 MHz loop in "normal" mode.

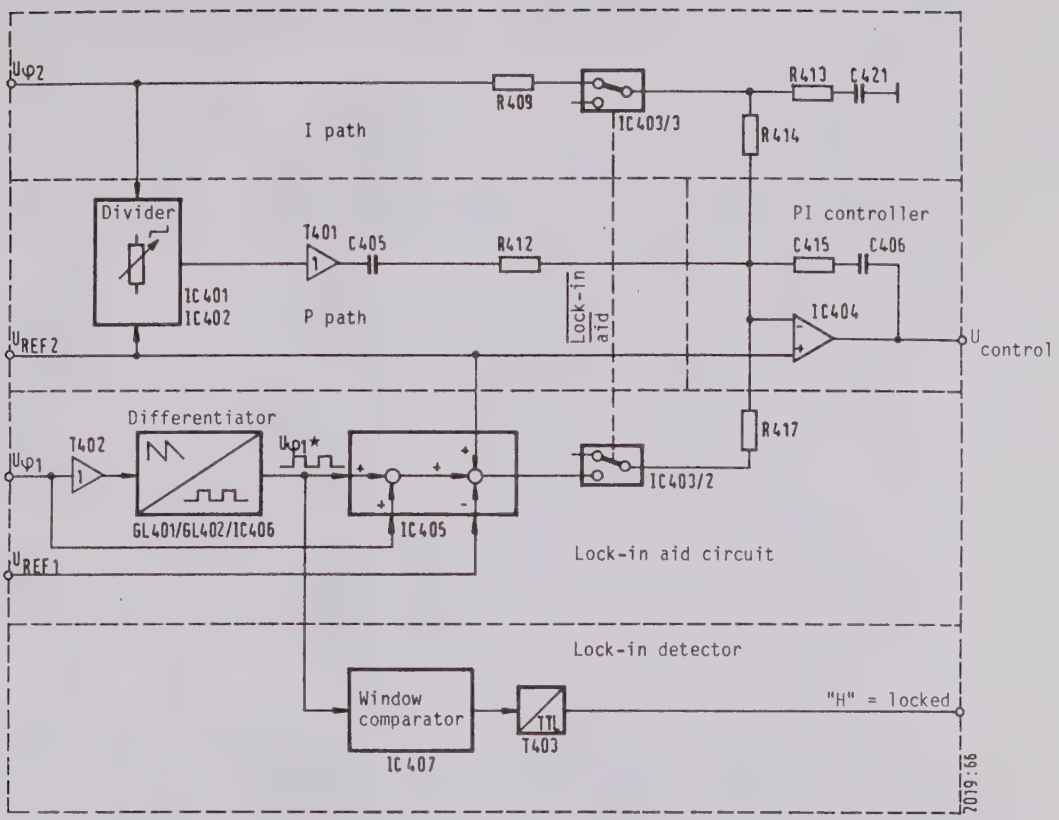


Fig. 9.2-28 Simplified block circuit diagram, Controller 2

Circuit branch description:

1. Divider paths for PI controller:

The I path consists of R 409, switch IC 403/3 and R 414. The staircase section R 413/C 421, together with R 409, reduces the gain in the I path. Switch IC 403/3 is used to disconnect the I path in "lock-in aid" mode.

The P path first includes a voltage divider comprising R 404 ... R 408, R 440 and R 441. The divider is based on U_{REF2}, C 424 ensuring an adequately low output impedance.

Analog switch IC 401 is used to set the division factor. A separate, undivided path via switch IC 402/2 is provided for a control limit frequency of 500 kHz (max. gain). When open, switch IC 402/1 disconnects the other divider path.

2. PI controller:

The control characteristics are determined by C 406, R 415 and the summation resistors R 412, R 414, R 415 and R 417 (for "lock-in aid"). The reference voltage is supplied via the filter section R 416/C 409. The combination R 439/Gl 403/Gl 404 limits the maximum control voltage span.

The total gain is determined by R 415 (alignment value for matching the gain to the steepness of the 220 MHz VCO).

When set to "lock-in aid", the output signal of the lock-in aid circuit is passed to the PI controller via R 417 and switch IC 403/2. The divider paths are inactive in this case. The P path is connected to U_{REF2} via IC 401, the I path being disconnected by IC 403/3.

3. Lock-in aid circuit:

In "normal" mode, this circuit, together with the lock-in detector, forms the lock-in check for the 11 MHz circuit. In "220 MHz lock-in aid" mode, it forms part of an "auxiliary" PLL, together with the PI controller.

The lock-in aid circuit is fed from the output signal $U_{\varphi 1}$ of the 11 MHz phase meter.

When unlocked, the latter provides a sawtooth oscillation.

The differentiating section C 412/R 426 downstream of buffer stage T 402 uses the sawtooth return edges to generate positive and negative pulses which are fed to buffer amplifier IC 406 via the holding sections Gl 401/C 413 and Gl 402/C 414. The amplifier output signal is passed to the lock-in detector and the summing amplifier.

In the summing amplifier, the original phase meter signal $U_{\varphi 1}$ (DC component) supplied via R 442 and R 421, is overlaid with the directional signals $U_{\varphi 1}{}^{*}$ (AC component) supplied via R 423 and related to the reference level U_{REF2} of the PI controller.

4. Lock-in detector:

The window comparator comprising IC 407 detects the pulses output by the lock-in aid circuit in unlocked state. A lock-in FF on the RF control is set via level converter T 403.

9.2.4.3 Sawtooth phase meter (STPM) [7/2019-0]

The STPM is an analog phase meter with S & H behaviour for an input frequency range from 0.7 MHz to 170 MHz. Due to the S & H behaviour, its gain is independent of the edge density of the input signal, this making it suitable for measuring the phase jitter of both clock and data signals.

Principle:

In sawtooth generation, a pulse generator is used to generate a short, high-amplitude pulse (approx. 1 ns, 5 Vp) from the sinusoidal regenerated clock signal supplied, this short signal charging a capacitor. In the intervals between the pulses, this capacitor is discharged via a current source which can be adjusted proportionally in relation to the bit rate, so that the phase meter steepness remains constant for all bit rates. A second pulse generator generates a switching pulse for a diode sampler from the edges of the input signal (data or clock), the sampler sampling the momentary voltage on the charging capacitor and storing it in a sample capacitor.

The sampled voltage is available with low impedance via a downstream buffer amplifier with FET input.

The theoretical measuring range of the phase meter of ±0.5 UI is limited to a minimum of ±0.25 UI by the charging time of the capacitor and by transients.

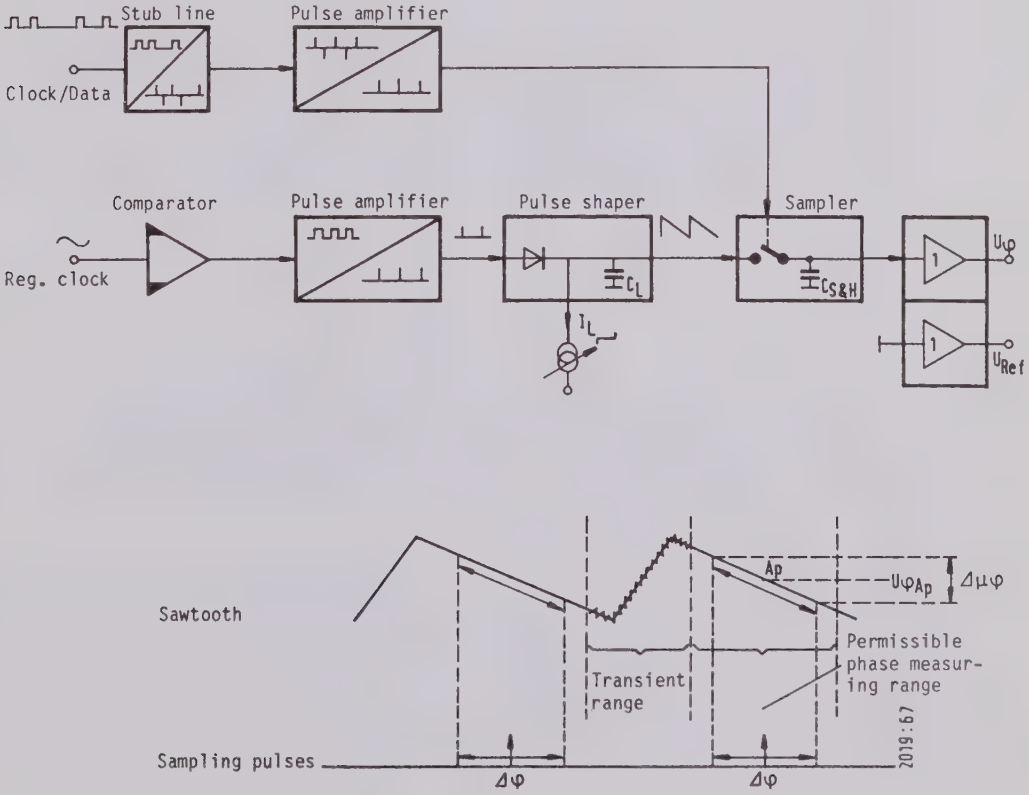


Fig. 9.2-29 Functional principle

Sampling pulse generator:

The stub line at the input of the sampling pulse generator forms positive and negative pulses with 2 ns pulse width from the edges of the ECL square-wave signal supplied by the input circuit.

The reference voltage of line receiver IC 301/1, which acts as a comparator, has a nominal value of -100 mV, meaning that only the negative pulse edges are processed.

The second stage IC 301/2 adjusts the driving signal for the downstream differential amplifier T 301/302 to a constant ECL span. The current source with T 317 is set to 30 mA.

Diode Gl 303 reduces the maximum Uce voltage of T 302 to permissible values and reduces its power dissipation.

In order to achieve an extremely short turn-on time, T 303 is driven with approx. 20 mA base current from T 302 at the time of turning on. Differentiator R 309/L 318 ensures that the high base current for T 303 only flows for a short time.

The downstream capacitor stages T 304, T 305 further increase the steepness of the pulse edges and are also driven with short, high-current pulses. Here, differentiation of the driving pulses is performed by C 307/L 319 and C 309/R 314.

A pulse edge with a rise time of less than 1 ns and a span of more than 10 V is available at the collector of T 305.

Sawtooth pulse generator:

The regenerated clock is fed to comparator IC 302 as a sinusoidal signal for conversion into a square-wave signal. The downstream pulse amplifier is roughly the same as that in the sampling branch. The essential difference is that a square-wave signal is present at the input in this case, rather than a 2 ns pulse. Differential amplifier T 306/T 307 is coupled capacitively, in order to be independent of the DC levels at the comparator outputs.

Sampler:

The sampling pulse is obtained by differentiation of the rising edge at the collector of T 305 and coupled into the sampling branch via transformer Ü 301.

The sampler is designed as a symmetrical 2-diode gate. A floating counter-voltage is built up by the sampling pulses across diode Gl 312 to ensure that the sampling diodes are reliably blocked during the intervals between pulses. C 328 and C 320 serve as charging capacitors for the counter-voltage and as coupling capacitors for coupling out the signal. DC coupling-out is achieved via R 343 and R 344. C 331 and C 327, together with the input capacitor of the FET follower T 316/1, represent the sampling capacitance.

Due to the symmetrical coupling-out with R 343/R 344 and C 328/C 330, only the voltage on the sampling capacitors is present at the input of the FET follower, while the voltage across Gl 312 is cancelled out. The symmetry alignment on C 327 ensures that the sampling pulses on the two transformer windings are synchronized.

Sawtooth pulse shaper:

The turn-on edge at collector T 310 is differentiated and coupled into the sawtooth pulse shaper by transformer Ü 302. R 330, Gl 307 on the primary side and R 334 on the secondary side are used to dampen the charging pulses and improve the linearity of the sawtooth ramp generated.

Gl 308 and Gl 309 switch through the charging pulse and are blocked during the intervals between pulses. Gl 306 limits the charging pulse. C 325 serves as a coupling capacitor, disconnecting the DC offset, while C 326, together with C 363 forms the charging capacitor for the sawtooth ramp.

The bit rate-proportional discharge current is fed via R 336.

The charging current is : I = 0.033 mA * fbit/Mbit

The nominal steepness is then: K = 0.127 V/rad

The current mirror with T 311 to T 313 and IC 303 is used to decouple the current source on the RF control (14) from the "hot" feed point into the sawtooth pulse shaper. C 332 and C 333 prevent interference from being coupled in from the charging pulses.

Buffer stage:

T 314, T 315 and T 316 make up two identical buffer stages with gain v = 1. The one acts as an impedance transformer for coupling out the sampled, phase-proportional signal voltage with high impedance, while the other generates a reference voltage, with which the operating point of the phase meter can be set on its characteristic.

The high input resistance of the buffer stage means that the discharging of the sampling capacitors is minimal, while the output resistance of the buffer stage is approx. 10 Ω.

The absolute level of the offset voltage at the U_{REF} and U_{PHASE} output varies from one unit to the next and may be between 1 and 3 V. The double FET T 316 means that the temperature drift of U_{REF} and U_{PHASE} is almost equal.
The drift of the set operating point thus remains slight. The operating point is set to the middle of the useful modulation range with P 302.

Operating voltage filter:

The +12 V operating voltage must be particularly free of interference. In order to minimize the current drop, despite the high current consumption, parallel control is provided with IC 6 via R 368. The lower limit frequency for adjustment is approx. 1.5 Hz. Interference up to a maximum of 50 mV_{pp} can be balanced out.

9.2.4.4 170 MHz low-pass filter [7/2019-T]

The input signal of the 170 MHz low-pass filter passes via a Chebishev low-pass filter of the 9th order (pass-band ripple < 2 dB, f_g = 168 MHz).

The output voltage of the filter is amplified by approx. 21 dB in a two-stage negative feedback amplifier (7 T 201, 7 T 202). The components 7 C 213 and 7 R 203 compensate for the frequency response of the overall circuit.

Transistors 7 T 203 and 7 T 204 decouple both outputs, which are matched to the characteristic impedance of the coaxial cables (Z_o = 75 Ω) with resistors 7 R 220 and 7 R 221.

This matching yields a voltage attenuation of 6 dB, resulting in a total voltage gain of the circuit of approx. +15 dB.

9.2.4.5 Mixer [7/2019-U]

The differential frequency between f_2 = 220 MHz (220 MHz VCO) and f_1 = 220.7 ... 387.2 MHz (frequency generator) is formed here. When the 220 MHz circuit is locked, this is then equal to the applied bit rate. Designation: Regenerated clock. Since a signal offset by 90° in relation to the sawtooth is required for data sampling on the code error card, a phase shift must take place at f_2 (constant frequency); consequently, 2 branches (2 mixers) are required.

Input f_1:

Source: Carrier oscillator, open-circuit voltage approx. +3 dBm, output impedance approx. 33 Ω. To switch through the mixer diodes (LO input), the signal of each mixer is amplified by voltage feedback and limited by the mixer diodes. Level at the LO input: 7 dBm ± 2 dB.

Input f_2:

Source: 220 MHz VCO, open-circuit voltage approx. +6 dBm, output impedance approx. 50 Ω. Due to interference products, the level in each branch is attenuated to -17 dBm. In branch 1 L 1, C 11 are used to attenuate 440 MHz because of interference products. In branch 2, the phase shift is generated with a low-pass filter of the second order.

Both IF signals are amplified to approx. -20 dBm (into 75 Ω) for further processing in the 170 MHz LP filter.

9.2.4.6 Buffer stage 2 [7/2019-W]

The heart of the circuit is the ECL comparator SP9685. Part of the inverted output signal is fed back to the inverting input, this resulting in positive feedback. The hysteresis is approx. 11 mV.

The input signal arrives from the 170 MHz LP filter (No. 2) with 0 to -8 dBm. The output signal is coupled out capacitively.

Output impedance: 75 Ω.

9.2.5 11 MHz CIRCUIT (E)

9.2.5.1 11 MHz phase meter [8/2019-G]

The 11 MHz phase meter consists of flip-flop IC 2/2, two pulse shapers IC 2/1 and IC 4, an 8 V controller (circuit around IC 1 and T 1) and a limiting amplifier T 2, T 3 and IC 3. The flip-flop with feedback IC 2/1 generates a pulse of about 2 ns width from the square-wave output signal of the 20:1 divider. The pulse width is determined only by the internal delay of the flip-flop. The square-wave output signal of the 11 MHz VCO is passed to gate IC 4/3 via coupling capacitor C 13.

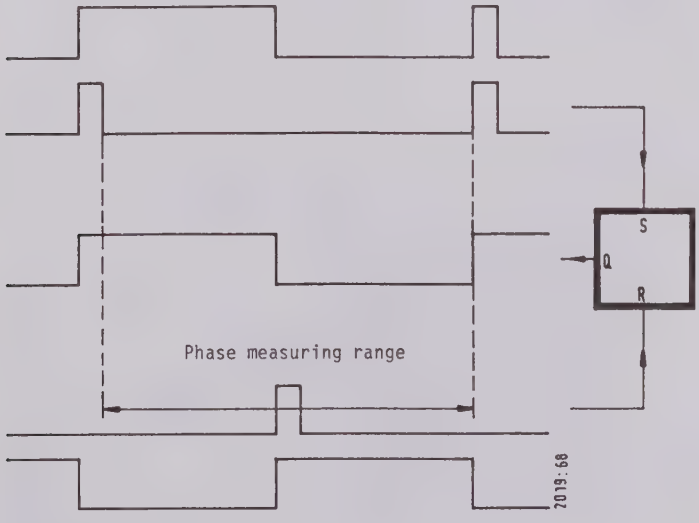
The delay of gate IC 4/2 is used to generate a roughly 2 ns wide pulse from the rising edges of the square-wave signal in this signal path as well. IC 2/3 is used to generate a voltage of about -1.3 V, half way between H and L, by adding the static H and L signals via the two resistors R 31 and R 33, this voltage determining the operating point of gate IC 4/3.

Pulse shaping in the SET and RESET branch of the phase meter flip-flop is necessary so as not to restrict the full measuring range of 360° too much (see Fig. 9.2-30). If the SET and RESET signal are both H, at the same time, the flip-flop is in an undefined state.

The square-wave output signal of flip-flop IC 2/2 is shifted by 3.3 V by Zener diode Gl 3 and thus matched to the differential amplifier IC 3/1 and 2. To increase the steepness of the output signal of this differential amplifier, the signal at the collector of IC 3/1 is passed via emitter follower T 3 to the base of transistor IC 3/2. Voltage divider R 17, P 2 and R 18 is used to set the operating point of the differential amplifier.

Since the measuring accuracy depends on the stability of the amplitude of the square-wave output signal, the output signal is limited by stable upper and lower thresholds. The upper limit (transistor IC 3/2 blocked) is the 8 V supply, which is controlled very accurately by voltage controller IC 1; the lower limit (transistor IC 3/2 switched on) is determined by the cathode voltage of diode Gl 4. A voltage of 4.4 V is present at the anode of diode Gl 4. Thus, limitation becomes effective at approx. 4 V. Transistor T 2 ensures that the voltage is available with very low impedance, while capacitor C 7 also filters out low spurious frequencies. The base voltage divider R 13 and R 14 sets the correct voltage at the diode.

The reference voltage required for the PI controller (in Controller 1) is generated by the voltage divider R 11, R 43 and R 44. In order to obtain the most similar temperature response possible for the reference and signal voltages, both signals are passed via identical emitter followers (IC 3/3 and IC 3/4).



Phase measuring range = ±144° ≙ 16 UI for the PJM-4 (due to 20:1 division)
1 UI ≙ 1 Unit interval = 360°

Fig. 9.2-30 Phase measuring range

9.2.5.2 Controller 1 [8/2019-H]

Normal mode:

Under normal circumstances, Controller 1 acts as a PI controller. Analog switch IC 3 is open and transistors T 2 and T 3 have high imedoance. The controller characteristics are determined by operation amplifier IC 1 with the associated components C 9, C 12, C 13, R 10 and R 7 and voltage divider P 2 and R 4.

Controller 1 clamp:

If the instrument is in CONTROLLER 1 CLAMP mode, the controller output (control voltage 1) is clamped by T 3 to a fixed voltage set on P 3. The control voltage can then be varied in the range from -3 V to +3 V. Operation amplifier IC 2/4 acts as a voltage divider and ensures a low-impedance voltage at transistor T 3. The FET T 3 is controlled by operation amplifier IC 2/3, which is wired as a comparator. If the digital signal at the non-inverting input is H, the control voltage of the 11 MHz VCO is clamped to the set fixed voltage; if the digital signal is L, the controller is in operation.

Lock-in:

In LOCK-IN mode, analog switch IC 3 is closed and capacitors C 9, C 12 and C 13 are re-charged to the voltage $U_{LOCK-IN}$ (connection 8 of the circuit) via operation amplifier IC 2/2.

SLOW:

If the controller is set to SLOW, the pass frequency of the entire 11 MHz loop is approximately 1 Hz. For locking-in, the controller is switched to FAST by transistor T 2. This sets the pass frequency of the control circuit to roughly 100 Hz. FET T 2 becomes conductive when switching from SLOW to FAST. Voltage divider P 2, R 4 and resistor R 7 are then bridged by resistor R 6. FET T 2 is driven by operation amplifier IC 2/1, which is wired as a comparator. The comparator threshold is set at 2.5 V by resistors R 14 and R 15.

Comparator IC 2/1 is designed in such a way that switching from FAST to SLOW takes place far more slowly than the other way round. When the fast/slow switching signal (connection 3 of the circuit) drops from H to L (SLOW -> FAST), the output of the comparator with the short time constant R 13, C 3 switches from 2 V to 12 V, since resistor R 9 is bridged by diode Gl 3. When switching from L to H takes place (FAST -> SLOW), the transition from 12 V to 2 V occurs at the output of the comparator slowly, since the time constant R 13 and R 9, C 3 is effective. Zener diodes Gl 1 and Gl 2 limit the span of the comparator output voltage to 2 V to 12 V. Resistor R 5 limits the current through the gate of FET T 2.

Capacitor C 2, together with trimmer P 1, ensures that the 11 MHz loop does not unlock again in the presence of large modulation when switching from FAST to SLOW.

If the gate of FET T 2 does not receive an AC voltage via C 2, the switching voltage of the FET is modulated by the AC voltage signal $U_{\varphi 1}$ and an equalization process in the form of an e-function is superimposed on the phase meter signal (see Fig. 9.2-31).

The fact that part of the AC voltage is passed to the gate of the FET reduces the level of modulation. If the AC voltage supplied is too high, an e-function in the opposite direction is produced (see Fig. 9.2-32).

The optimum lock-in range is obtained when the first sine wave after switching over has the same height as the signal after settling (see Fig. 9.2-33).

The measuring result of the phase meter $U_{\varphi 1}$ arriving at the circuit is also supplied to Controller 2 via buffer stage T 1 ($U_{\varphi 1}$).

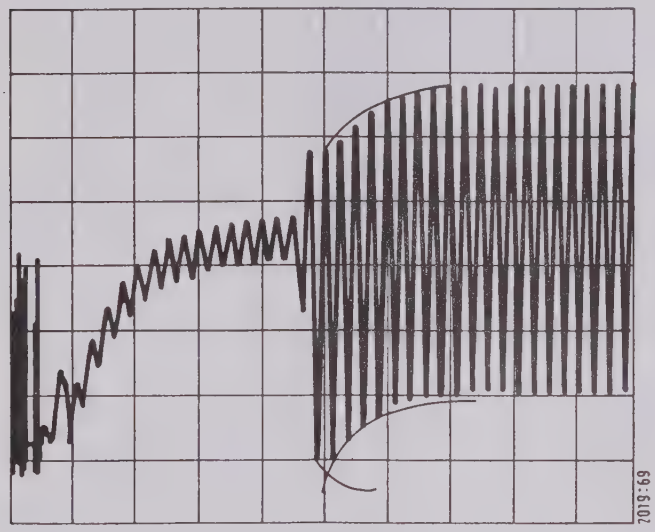


Fig. 9.2-31 Misalignment, Controller 1

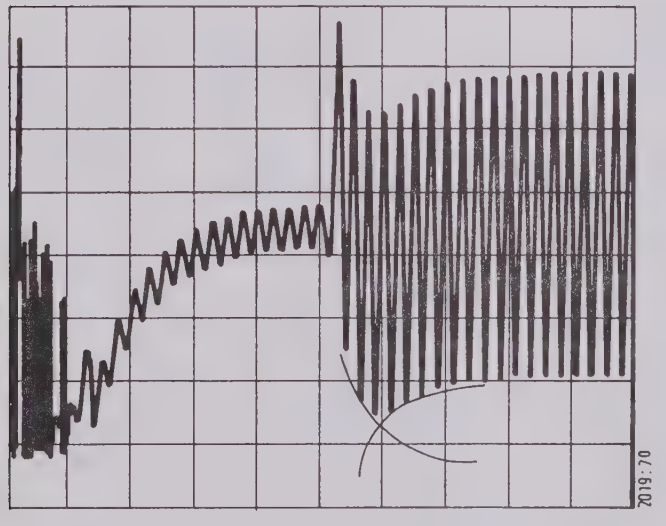


Fig. 9.2-32 Misalignment, Controller 1

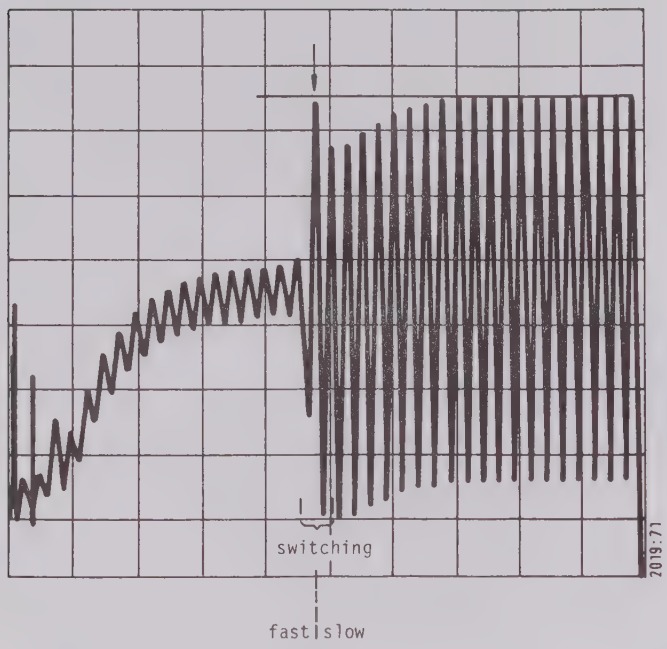


Fig. 9.2-33 Overall lock-in process, 11 MHz loop. Controller 1 correctly aligned.

9.2.5.3 11 MHz VCO [8/2019-J]

The 11 MHz VCO is a crystal oscillator with Hartley circuit. The tank circuit consists of crystal Q 101, capacitance diodes G1 101 to G1 104 and capacitors C 105, C 104 and C 112. The frequency range of the VCO is between 10.998 and 11.002 MHz with a tuning voltage between -4 V and +4 V. Crystals with a nominal frequency of 10.9985 MHz had to be used in order to obtain a frequency of 11 MHz with the capacity profile of the diodes as a function of the tuning voltage at 0 V control voltage.

The signal for the amplitude controller (transistors IC 102/1 and 2) and the limiter amplifier (transistors IC 102/3 and 4) is tapped at the emitter of oscillating transistor T 101.

The amplitude controller sets the base voltage of oscillating transistor T 101 in such a way that an AC voltage of 0.5 V_{pp} is present at the emitter. The signal is amplified by transistor IC 102/2 and then rectified by diode G1 105. If the amplitude of the oscillator increases, the base voltage of transistor IC 102/1 rises, the emitter-to-collector junction assumes a lower impedance, the base voltage at oscillating transistor T 101 drops and the amplitude becomes smaller.

The limiting amplifier consists of the symmetrical differential amplifier IC 102/3 and 4 and generates a square-wave signal with ECL span (0.8 V_{pp}) at the collector of transistor IC 102/4, which is coupled out to the 11 MHz phase meter via emitter follower IC 102/5. Since the VCO must have very little noise (down to less than 1 Hz!), the voltage on which capacitance diodes G1 101 to G1 104 are based is controlled by voltage controller IC 101 and additionally filtered with the low-pass filter R 122, C 113.

9.2.5.4 20:1 divider [8/2019-AM]

The output signal of the 220 MHz oscillator, capacitively decoupled by capacitor C 101, is first divided by four in IC 101. The output of IC 101 already has ECL level and is thus directly connected to the input of IC 102, which divides the signal by five.

The LC tank circuit L 101, C 105 filters the 220 MHz components out of the output signal of the 20:1 divider.

Resistor R 102 and the input capacitor of the 11 MHz phase meter form a low-pass filter for damping the tank circuit L 101, C 105.

9.2.5.5 11 MHz filter [8/2019-AN]

The 11 MHz filter is a low-pass filter with a cutoff frequency of 5.5 MHz and two attenuation peaks at 11 MHz and 22 MHz. It converts the change in pulse width of the phase meter output signal into a voltage change.

The reference voltage U_{REF1} is looped from the phase meter through the 11 MHz filter to Controller 1.

9.2.6 ADDER (F) [10/2019-AF]

Principle:

The output signals of the sawtooth phase meter and the 11 MHz phase meter are added with the correct amplitude and phase in the adder.

For addition with the correct phase, the different phase responses of the two PLL circuits must be simulated in the adding paths.

A variable delay element in the 220 MHz path equalizes the difference in delay between the circuits. It is followed by a low-pass filter which simulates the phase response of the 11 MHz filter.

The modulation and bit rate frequency-dependent phase response of the sawtooth phase meter must be simulated in the 11 MHz path. This phase response is caused, among other things, by the S & H behaviour of the sawtooth phase meter and can be described by several time constants, most of which are dependent on bit rate.

This phase response is simulated in the 11 MHz path by a voltage-controlled low-pass filter of the 2nd order, whose cutoff frequency can be set proportionally to the bit rate frequency.

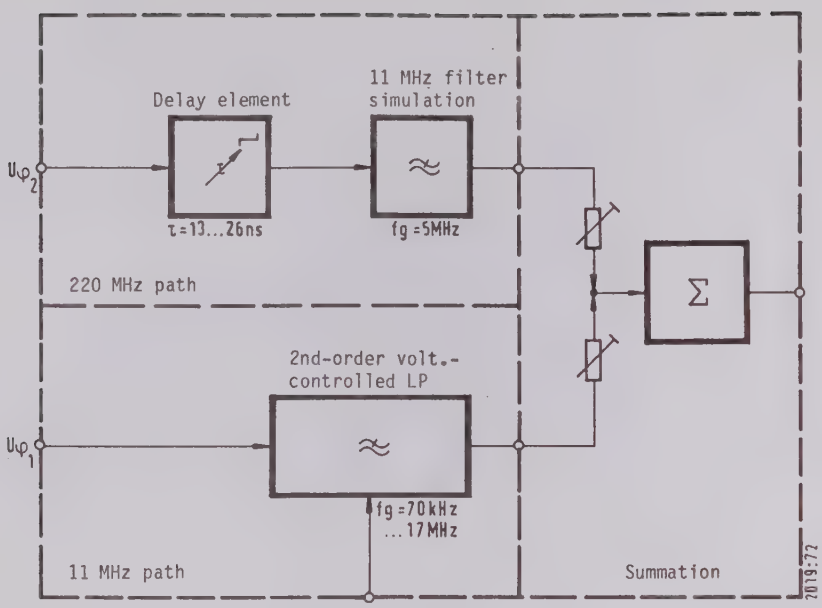


Fig. 9.2-34 Block circuit diagram

220 MHz path:
The output signal $U_{\varphi 2}$ of the 220 MHz circuit is passed via a buffer stage to a delay network comprising L 1 ... L 6 and C 4 ... C 10. S 1, S 2 and S 4 can be used to set the delay time between 12.7 and 25.6 ns in steps of 4.3 ns.

The 11 MHz filter is simulated by C 11 ... C 18 and L 7, L 8. R 5 and R 6 are the terminating resistors for filter and delay network.

P 102 is used to set the summation gain for the 220 MHz path, trimmer C 128 being used to correct the frequency response.

11 MHz path:
The output signal $U_{\varphi 1}$ of the 11 MHz circuit is passed to the voltage-controlled active low-pass filter comprising T 10, T 11, T 104, T 105 and IC 101.

The two voltage-controlled current sources IC 10/1, T 13 and IC 10/2, T 12 supply symmetrical control currents between 2.9 and 681 µA, derived from the bit rate-proportional control voltage U_{LP}, for controlling the differential resistance of transistors T 10, T 11 and T 104 and T 105, which are wired as diodes.

The parallel circuits of the differential resistors through coupling capacitors C 132, C 101 and C 102 form the two controllable resistors in the input branch of the active LP. Feedback for the 2nd-order LP takes place via C 131 and C 129.

The basic cutoff frequency can be set with trimmer C 104.

P 101 is used to set the summation gain for the 11 MHz path.

S 4 can be used to switch off the 11 MHz path for test purposes.

Summing amplifier:
The summing amplifier is largely identical to the 30 dB amplifier in the peak rectifier [2019-AH].

9.2.7 FILTER (H) [11/2019-Y]

9.2.7.1 Block circuit diagram

The demodulated jitter signal is fed in via comb Pt. 12 c of the filter card. After being filtered via a high-pass/low-pass combination, it is passed to the following circuits:

a) via 9 c to the demodulation output socket (front panel)
b) via Pt. 1 to peak rectifier (12)
   and after further processing to hit counter (13)
c) to peak rectifier (12) for jitter evaluation.

Each path has a second-order HP filter of 1.83 Hz (-3 dB point).

Furthermore, a third-order low-pass filter of 4.5 MHz (pass band) limits the high-frequency end of the bandwidth in all three paths. The separation into a second-order low-pass on the filter card and the third-order filter in the individual signal branches has advantages in terms of noise. The third-order filter (first-order element, bandwidth 5 MHz) is in each case positioned downstream of the last amplifier (hit counter path and jitter path).

The low-pass and high-pass filters can be combined as desired. When the 4.5 MHz low-pass is switched on, only the common 4.5 MHz LP is in the measuring path. Using the low-pass selector switch, the resistors R provide only 6.02 dB attenuation of the signal. If the 1.83 Hz high-pass is selected, the measured signal is passed through directly, reaching the common 1.83 Hz high-pass filter effective for all paths.

A filter with 75 Ω output impedance can be looped in via sockets Bu 1 and Bu 2. The internal filters are then bypassed. Variations of the external filter of ±1 dB can be corrected with P 1.

9.2.7.2 Selectable low-pass filters

The individual low-pass filters are third-order low-passes in a circuit. Except on the 40 kHz low-pass, each is preceded by an emitter follower stage 11 IC 8, which decouples the sections from the input capacitance of change-over switch 11 IC 1. 11 R 12 and 11 R 18 merely divide the signal by 2 when set to the 4.5 MHz position. No filtering takes place. Depending on how change-over switch 11 IC 1 is driven at A, B and C, it switches one of its input signals through (see Table in circuit diagram (11)). The associated trigger signal for switching is the $\overline{D\emptyset}$ signal (see Section 9.2.7.7).

9.2.7.3 Selectable high-pass filters

The individual high-pass filters each consist of a first-order RC section. The analog change-over switch 11 IC 4 selects the capacitor via which the signal is to be passed, while 11 IC 2, 11 IC 3 or 11 Rel 1 switches the corresponding resistor to chassis. No filtering take place when the 2 Hz setting is selected; the signal is switched through directly. The relationship between the signals as a function of filter setting and high-pass filter selection is shown in the Table in the filter circuit diagram (11). The trigger signal used for switching is $\overline{D8}$.

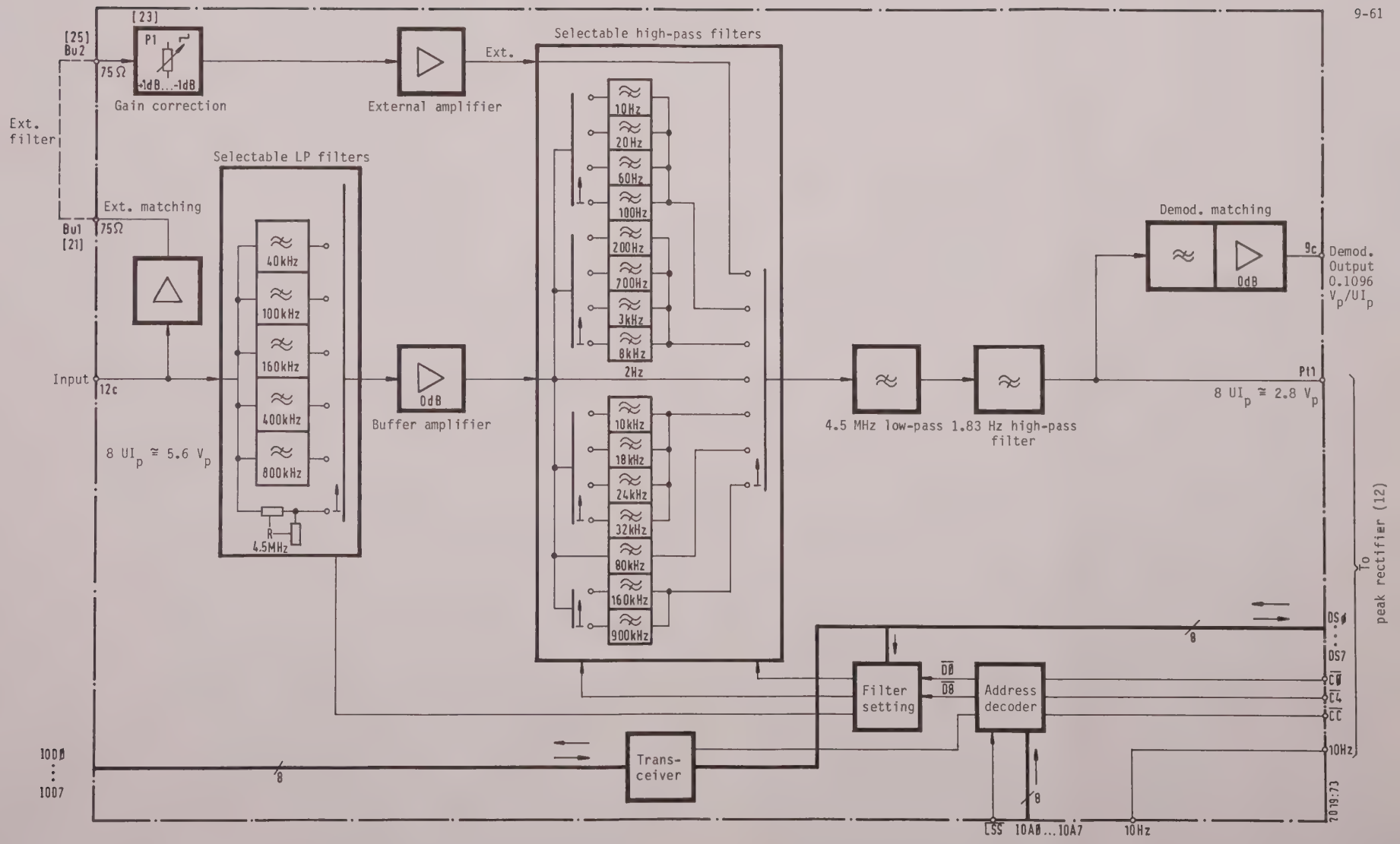


Fig. 9.2-35 Block circuit diagram, filter (11)

9.2.7.4 External filter

The internal filters can be bypassed when set to external. A filter can be looped into the measuring path via sockets 11 Bu 1 and 11 Bu 2. The bandwidth limitation of 1.83 Hz and 4.5 MHz remains effective even when using the external filter. Both sockets have an output impedance of 75 Ω. The fundamental filter attenuation of 6 dB can vary by ± 1 dB. This deviation can be corrected by alignment with 11 P 1.

Signal path:

The jitter signal from comb Pt. 12 c is divided and passed via the emitter follower 11 T 3 to 11 Bu 1. Division is performed by 11 R 10 and 11 R 30. 11 C 41 raises the frequency response. The combination 11 R 62 and 11 C 40 corrects a frequency response caused by External amplifier [2019-AD].

The signal from 11 Bu 2 passes via 11 P 1 and External amplifier [2019-AD] to multiplexer 11 IC 4.

9.2.7.5 4.5 MHz low-pass, 1.83 Hz high-pass

The low-pass is formed by the second-order section comprising 11 R 65, 11 L 6, 11 C 29 and 11 C 31, downstream of the emitter follower (11 T 4).

The high-pass consists of transistor 11 T 6, wired as a source follower, buffer amplifier [2019-AB], 11 IC 7, wired as an integrator, and the RC section 11 R 68, 11 C 30. The output voltage of the buffer amplifier is fed back to the input of the source follower via the integrator and the RC section, and is regulated to 0 V. The transmission characteristics between the input of the source follower at 11 R 69 and the output 11 Pt. 1 correspond to those of a second-order high-pass with a cutoff frequency of 1.83 Hz.

9.2.7.6 Demodulator output

The filtered jitter signal is passed to the front panel socket via emitter follower 11 T 7. The output impedance is 75 Ω.

The steepness of the output with 75 Ω termination is aligned to 0.1096 V_{pp} per UI_{pp} with 11 P 2. 11 C 37 is used for frequency response alignment.

9.2.7.7 Address decoder, transceiver

The address decoder consists of four 1-out-of-4 decoders (11 IC 7, 11 IC 8). If one of the hexadecimal numbers CØ, C4, C8, CC, DØ or D8 appears on the I/O address bus as a binary code word, the $\overline{LSS}$ pulse (active LOW) generated by the microprocessor is transmitted on the corresponding output line $\overline{C\emptyset}$, $\overline{C4}$, $\overline{C8}$, $\overline{CC}$, $\overline{D\emptyset}$ or $\overline{D8}$ (see Table in circuit diagram (11)). The two least significant digits IOA0 and IOA1 are not evaluated.

11 G1 10, 11 G1 12 and 11 R 141 together act as an AND gate, which derives the signal for reversing the direction in transceiver 11 IC 16 from the two signals $\overline{C\emptyset}$ and $\overline{C4}$. $\overline{C\emptyset}$ and $\overline{C4}$ cause the A/D converter of peak rectifier (12) to output data. Consequently, if $\overline{C\emptyset}$ = LOW or $\overline{C4}$ = LOW, the transceiver must be switched through in B --> A direction.

The filter setting is used to store the microprocessor data intended for switching the high and low-pass filters. A pulse occurring in parallel on $\overline{D\emptyset}$ or $\overline{D8}$ (active LOW) from the address decoder causes the data to be stored in the appropriate module. The individual high and low-pass filter involved is then set in accordance with the Tables in circuit diagram (11), Filter.

9.2.7.8 Buffer amplifier; external amplifier

a) Buffer amplifier:

This amplifier operates as a buffer stage with a gain of 1. The advantage of this kind of amplifier is the high input impedance and low output impedance. Transistor T 101 operates as an emitter follower. It is fed back with T 102. The ring gain is roughly 30 times. The output impedance, measured at Pt. 7 on card [2019-AB], is approx. 0.1 Ω. The input impedance at Pt. 1 on [2019-AB] is roughly

$V_{ring} \cdot \beta_{(T101)} \cdot R_L$

V_{ring} = Ring gain

R_L = Load resistance at card Pt. 7 [2019-AB]

The RC section R 105, C 103 attenuates the gain towards higher frequencies.

b) External amplifier:

This amplifier essentially operates in the same way as the buffer amplifier. Its gain from Pt. 1 to Pt. 8 is roughly $1 + \frac{R\ 207}{R\ 209} = 3.1$ (card [2019-AD]).

9.2.8 PEAK RECTIFIER (K) [12/2019-Z]

9.2.8.1 Block circuit diagram (see Fig. 9.2-37)

The peak rectifier can measure the positive and negative peak value. Its dynamic range is 84 dB (2.8 V_p to 177 μV_p at Pt. 1). In the level plan, 2.8 V_p is defined as 0 dB.

The 30 dB amplifier is switched into the signal path in accordance with the level at Pt. 1. Furthermore, an attenuation of 10 dB, 20 dB and 30 dB can be achieved with the 10 dB and 20 dB dividers. This is controlled by the microprocessor via the divider controller. The signal passes to the two peak value meters $-\tilde{u}$ and $+\tilde{u}$ via the peak rectifier amplifier.

Measurement of the positive and negative peak value takes place in two separate networks in a 5 Hz cycle controlled by the pulse generator. The positive and negative peak values are alternately passed to the A/D converter via the holding element in a 10 Hz cycle, then reaching the data lines DS 0 ... DS 7 as a data signal. The pulse generator controls transfer into the holding element and triggers the A/D converter for the conversion cycle. It also shows whether a positive or negative peak value is present at the input of the A/D converter. Among other things, the 10 Hz signal is used to synchronize the microprocessor for receiving the data from the A/D converter. This transfer takes place in two cycles and is controlled by the signals $\overline{C\emptyset}$ and $\overline{C4}$. $\overline{CC}$ causes the data to be transferred from the microprocessor to the divider controller, which then makes the corresponding settings. The overload monitor shows when the positive or negative peak value exceeds a level of 3.5 V.

Using this signal and the measurements of the peak rectifier, the microprocessor determines the aforementioned gain, selectable in 10 dB steps, via the divider controller. The mode of operation of this controlled gain setting is shown in Fig. 9.2-36.
Switching between the individual gain stages takes place with a hysteresis of ±1.5 dB. At the maximum gain of +60 dB, the level range at the input of the peak value meters at 12 TP 1 is -24 dBr to +1.5 dBr.

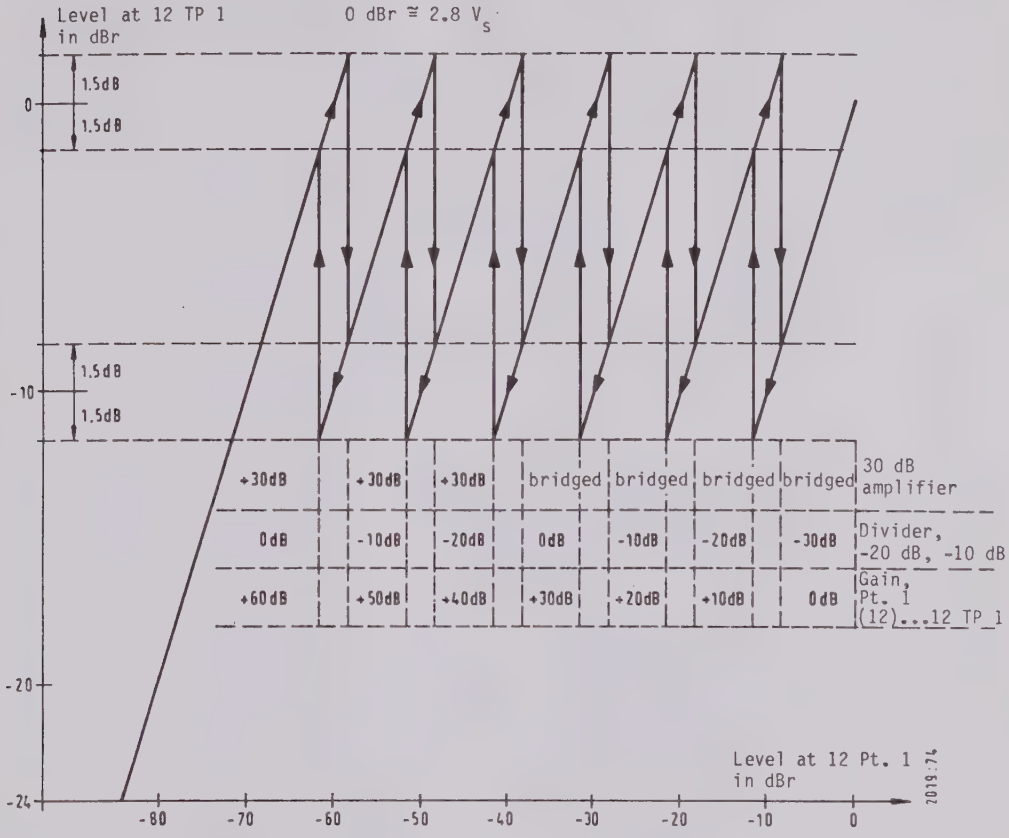


Fig. 9.2-36 Gain setting on the peak rectifier

The signal to the hit counter passes via the 1/16, 1/4 dividers and the hit counter amplifier (v = +21.16 dB). The divider can be set in stages of 1/1, 1/4 and 1/16 via the divider controller. For division by 1/6, 8 UI ≅ 2.0 Vp applies for the signal at (12) Pt. 5.

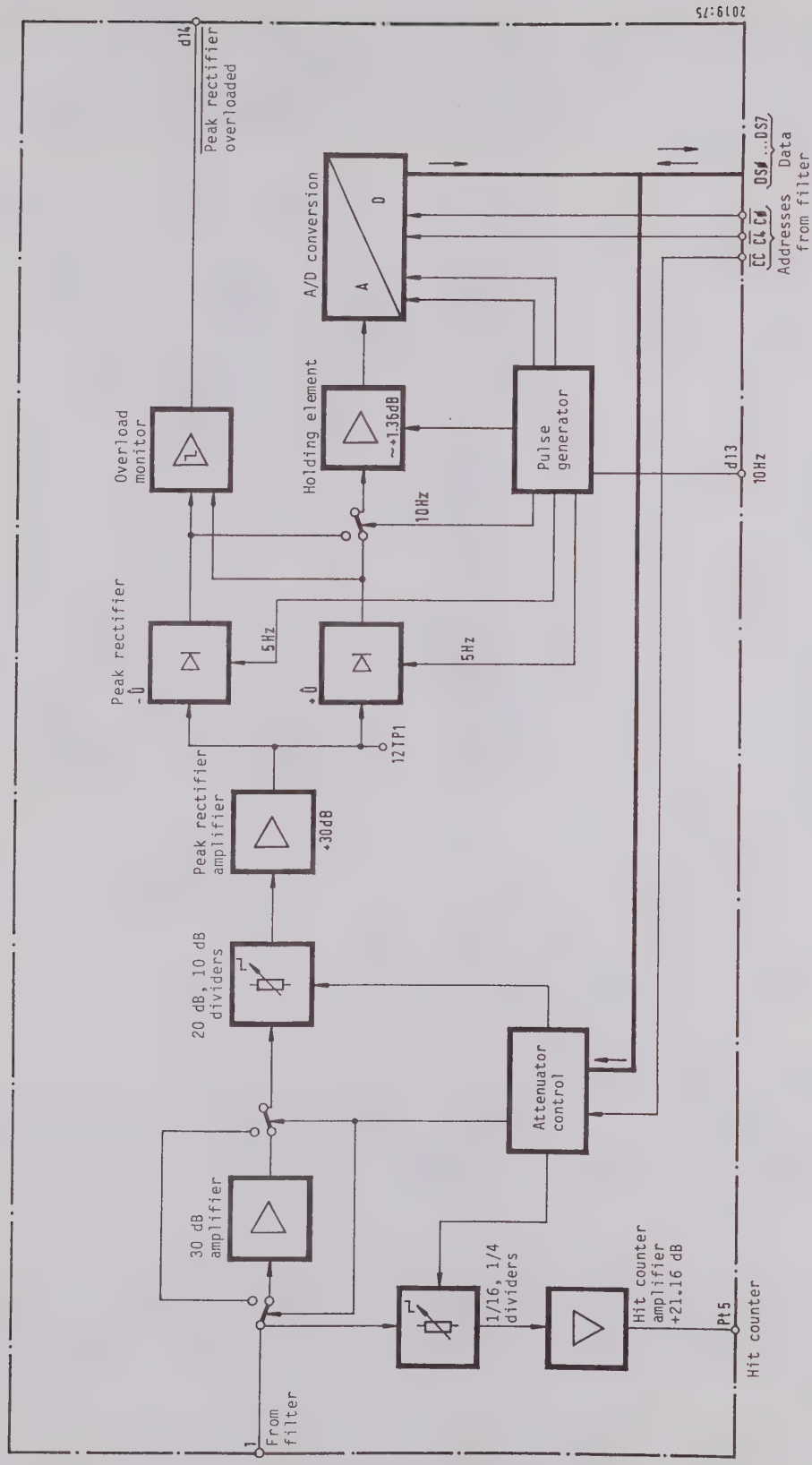


Fig. 9.2-37 Block circuit diagram, peak rectifier

9.2.8.2 30 dB amplifier [12/2019-AH]
Hit counter amplifier [12/2019-AJ]
Peak rectifier amplifier [12/2019-AG]

These three amplifiers are essentially identical. Each is accommodated on a separate board [2019-7031] and composed of SMD components. The circuits can be regarded as operation amplifiers wired as positive amplifiers.

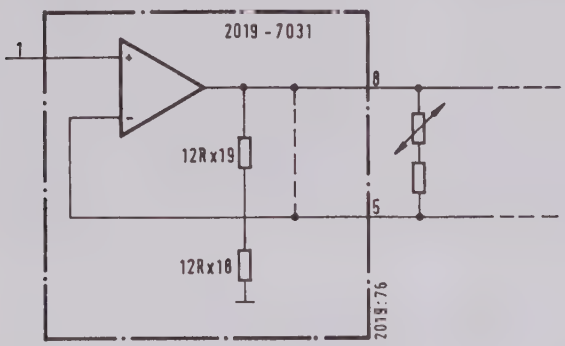


Fig. 9.2-38 Amplifier [2019-7031]

The feedback from the output Pin 8 to the "-" input Pin 5 determines the gain. The external wiring of the amplifiers between Pin 8 and Pin 5 with a PTC resistor and a series resistor on board [2019-Z] is designed to compensate for the temperature coefficient of the amplifiers. The hit counter amplifier [2019-AJ] also takes the temperature coefficients of the upstream source follower stages (11 T 6, 12 T 2 and 12 T 1) into account.

The amplifiers themselve consists of a differential amplifier (12 IC X01/1, 12 IC X01/2), with an emitter stage with current feedback (12 T X01) connected to its inverting output. 12 IC X01/3 and 12 IC X01/4 are both wired as emitter followers. A transistor current source (12 IC X01/5) acts on the emitter on the voltage follower on the output side. Trimmer C X05 is used to correct the frequency response. The hit counter amplifier and peak rectifier amplifier are additionally fitted with capacitor 12 C 308 and 12 C 408, respectively. This causes both amplifiers to act as first-order low-pass filters, supplementing the 4.5 MHz low-pass filter in circuit diagram (11), filter (see Section 9.2.7).

9.2.8.3 Peak value meters, overload monitor

The two peak value meters $+\hat{U}$ and $-\hat{U}$ essentially each consist of a comparator (12 IC 6, 12 IC 7) and an integrator (12 IC 8/1/2). They only differ in that the comparator inputs are reversed on peak value meter +U and that the output voltage of its integrator is inverted when fed back to the comparator (12 IC 8/2). The output voltages at 12 IC 8, Pin 8 and Pin 14, have the negative value of the corresponding peak value at the end of a measuring cycle.

The comparator compares the output voltage of the integrator with the momentary input voltage at 12 TP 1 and, if necessary, loads capacitor 12 C 15 (or 12 C 16) via 12 Gl 6 and 12 R 41 (or 12 Gl 7 and 12 R 43) until the integrator voltage matches the input voltage on the comparator. If the comparator output $\overline{Q}$ = LOW, the output voltage on the integrator remains unchanged. The potential at the "+" input of the integrators is selected in such a way that 12 Gl 6 (or 12 Gl 7) reliably cuts off in this case. Diodes 12 Gl 1, 12 Gl 2 and 12 Gl 3, 12 Gl 4 prevent the input voltage range of the comparators from being exceeded. The integrators are discharged with approx. 3.4 mA for a period of 1 msec. in a 5 Hz cycle via 12 T 3 and 12 T 4. The discharge transistors are driven by the pulse generator. The output voltage of the integrator is transferred to the holding element immediately prior to discharging (see Section 9.2.8.5). The charging of the integrator up to the peak value of a periodic input signal is shown in Fig. 9.2-39.

The overload monitor consists of the two comparators 12 IC 16/1/2. The overload signal goes to LOW state if one of the two output voltages of the peak value meters drops below a voltage of -3.5 V, i.e. if a peak value exceeds the level of 3.5 V.

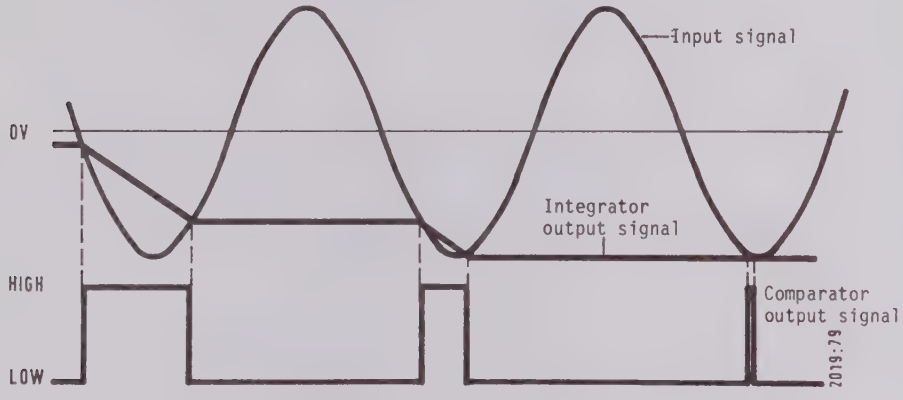


Fig. 9.2-39 Negative peak value meter

9.2.8.4 Holding element

The holding element is used to decouple the A/D converter from the peak value meters. The pulse generator switches through 12 T 5 for 1 ms periods in a 10 Hz cycle. During this time, 12 C 20 is charged to the voltage value at 12 IC 8, Pin 1. When 12 T 5 cuts off, the voltage at 12 C 20 is maintained. A/D conversion in 12 IC 14 takes place during this time.

12 IC 8/4 acts as an inverting amplifier, whose input signal is switched between the positive and negative peak value by 12 IC 9/1 in a 5 Hz cycle. The gain is approx. -1.17. 12 P 2 and 12 P 3 can be used to equalize differences in gain between the two peak value meters, as well as for alignment of the overall gain between the input of filter (11) 12 c and peak rectifier (12), including A/D converter. 12 P 4 and 12 P 5 are used to correct the offset voltages on the peak rectifier amplifier, the two peak value meters and the holding element.

9.2.8.5 Pulse generator

In the pulse generator, the 4.096 MHz signal of the crystal oscillator is first divided at a ratio of $1:2^{13}$ to form a symmetrical square-wave signal of 500 Hz and then again divided twice at a ratio of 10:1 by two Johnson counters. The output signals of the Johnson counters are square-wave signals with a 1:10 mark-to-space ratio. A combinatorial network forms the individual control signals. The relationships are shown in the following timing diagram.

9.2.8.6 A/D conversion

A/D conversion takes place in 12 IC 14, a binary 12-bit converter operating by the dual-slope integration method. It assigns the digital value 4000 to a peak value of +1.5 dBr (= 3328 mVp), i.e. it has a resolution of 0.832 mV. A conversion cycle is started by a trigger pulse from the pulse generator at RUN/$\overline{\text{HOLD}}$ (see Fig. 9.2-40) and lasts a maximum of 75 msec. Data transfer to the I/O data bus is controlled by the two address signals $\overline{\text{C0}}$ and $\overline{\text{C4}}$. It takes place in "Direct Mode" in two stages.

1st stage: $\overline{\text{C0}}$ = LOW. Data B 9 to B 12 ("High Byte"), OR (Overrange) and POL (Polarity) are switched through and the outputs of data B1 to B8 ("Low Byte") have high impedance. At the same time, the signalling signal is switched through via 12 IC 9/3 by the pulse generator.
Here: DS 7 = HIGH - positive peak value
DS 7 = LOW - negative peak value

2nd stage: $\overline{\text{C4}}$ = LOW. Data B1 to B8 are switched through and the outputs of data B9 to B12, POL and OR have high impedance.

When $\overline{\text{CE/LOAD}}$ = HIGH, all data outputs of the A/D converter have high impedance. The A/D converter can only be read while the 10 Hz signal is HIGH. The microprocessor adapts to the 10 Hz signal accordingly for polling.

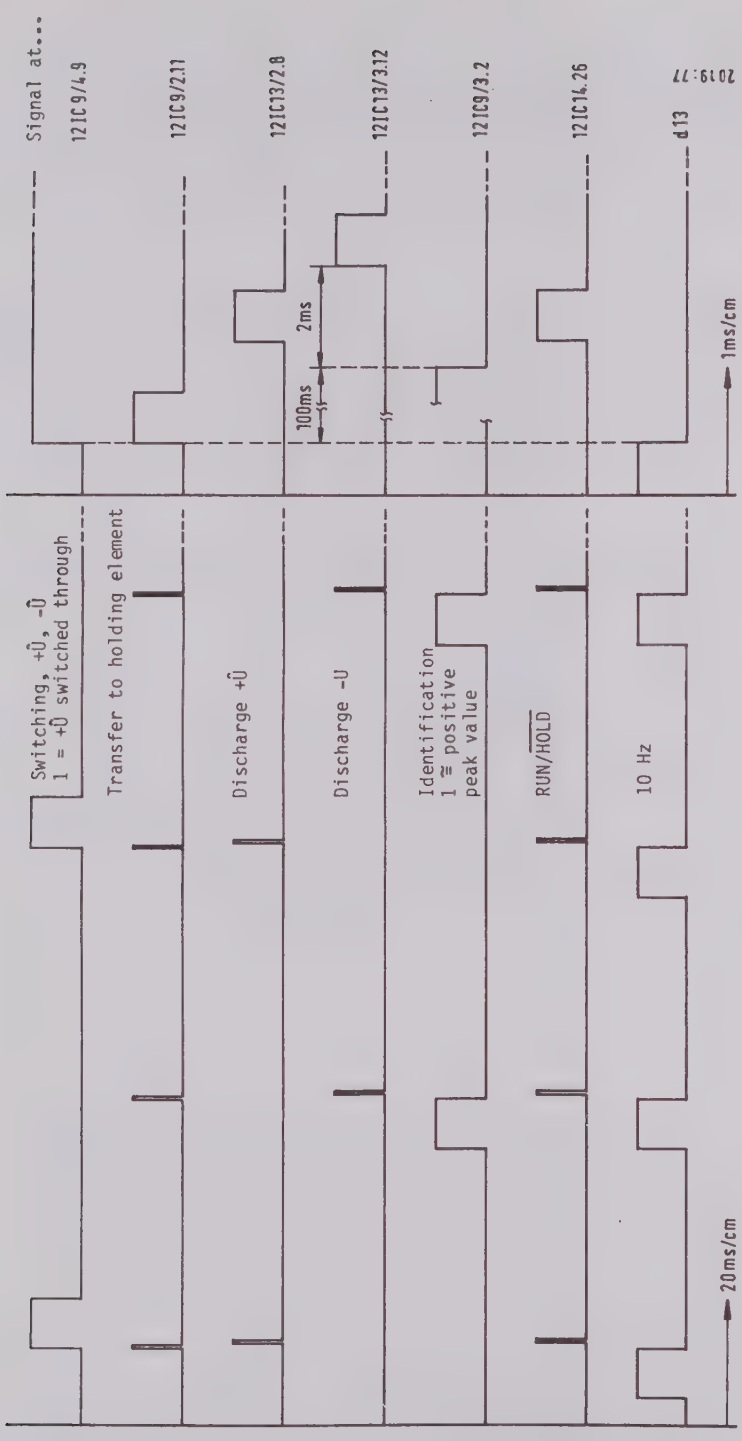


Fig. 9.2-40 Timing diagram of pulse generator

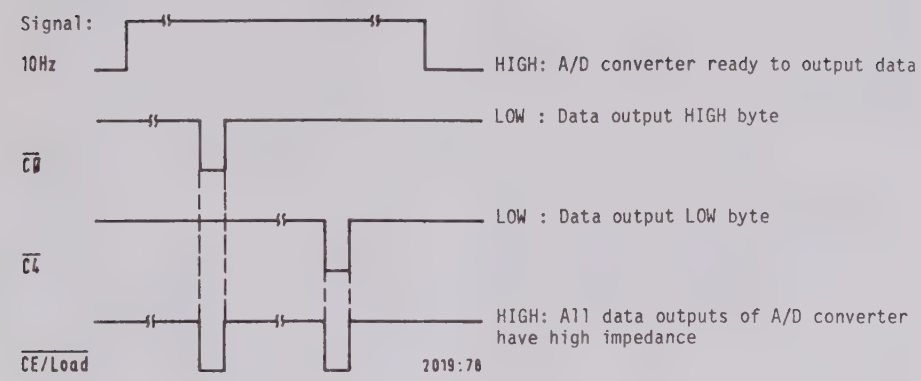


Fig. 9.2-41 Data polling on the A/D converter

9.2.8.7 Divider controller

A LOW pulse of the CC signal causes the divider controller to transfer the data at DS0 to DS5 into D-flip-flop 12 IC 2, where they are available as static output signals. The individual relays are then switched via the inverting driver stage 12 IC 1.
The following assignments apply:

HIGH state at 12 IC 2:	Activated relay, No. ...	Function	
Q 0	1	30 dB amplifier bypassed	
Q 1	2	-20 dB, -10 dB dividers:	-20 dB partial attenuation
Q 2	3		-10 dB partial attenuation
Q 3	4	1/16, 1/4 dividers:	1/4 division
Q 4	5		1/16 division

Fig. 9.2-42 Divider control

Further Tables can be found in circuit diagram (12).

9.2.8.8 Hit counter amplifier, 30 dB amplifier, peak rectifier amplifier

The three amplifiers are essentially of identical design. They differ only as regards their individual gains:

Hit counter amplifier: + 21.16 dB between 12 rel 4, Pin 4, and (12) Pt. 5
30 dB amplifier : + 30.0 dB between 12 rel 1, Pin 4, and 12 rel 1, Pin 3
Peak rectifier gain : + 30.0 dB between 12 rel 3, Pin 4, and 12 TP 1

The gains are determined by amplifiers [2019-AH/AG/AJ]. The 30 dB amplifier has no source follower input stage; in addition, its gain can be aligned by means of 12 P 1. The following description is based on the peak rectifier gain.

Transistor 12 T 2 is wired as a source follower and is used for decoupling, since the upstream divider must not be loaded. The actual amplifier stage is coupled capacitively via 12 C 44. Its input voltage is regulated to 0 V by integrator 12 IC 5. The voltage divider 12 R 28, 12 R 100 reduces the ring gain in order to prevent oscillation of the control circuit. Due to this input voltage control, the lower limit frequency of the gain is approx. 0.5 Hz.

9.2.8.9 -20 dB, -10 dB divider

The divider consists of two voltage dividers which can be bypassed by means of 12 rel 2 and 12 rel 3 or connected in series. They are dimensioned in such a way as to yield an attenuation of 0 dB, 10 dB, 20 dB or 30 dB, depending on the switch settings (see Table in circuit diagram (12)). 12 C 4 is used to compensate for the frequency response and compensates for circuit capacitances of the components.

9.2.8.10 1/16, 1/4 divider

The 1/16, 1/4 divider is a voltage divider which can be bypassed by means of 12 rel 4 and 12 rel 5 or tapped for division by 1/4 or 1/16 (see Table in circuit diagram (12)). Components 12 C 45, 12 C 46 and 12 R 13 are used for frequency response compensation.

9.2.8.11 Voltage supply

The peak rectifier board [2019-Z] is supplied with the following voltages:

+11 V at d 15 ; -11 V at (12) Pt. 7
+12 V at (12) Pt. 3; -12 V at (12) Pt. 6
+5 V at (12) Pt. 4; 0 V at (12) Pt. 2

The +6.9 V voltage is additionally generated from the +12 V via 12 Gl 5. 12 T 6 is used to generate the -7.5 V from -12 V. Some of the individual modules are supplied directly, other via separate filters.

9.2.9 HIT COUNTER (I) [13/2019-AA]

A distinction can be made between three assemblies on the hit counter:

a) Frequency counter

b) Phase hit counter

c) Real-time clock

Description of a):

The input signal of the frequency counter is the regenerated clock which, arriving from low-pass filter 1, must be present at Pin 3/IC 1 with at least 125 mV peak. Downstream of the comparator and a 10:1 divider (IC 2) comes the 24-bit counter, after a multiplexer. The counter is inhibited and enabled by the 10 Hz clock and reset by the processor. The external clock divided by 10 can also be counted via the multiplexer (IC 3).

Description of b):

With the aid of the inverter (IC 19), the 12-bit D/A converter (IC 18) applies the analog voltage to be compared to the two comparators. With the demodulated signal at both comparators, IC 21 indicates the positive transgressions of the phase threshold and IC 20 the negative transgressions. IC 22/23/24 turn this into a pulse of at least 40 ns duration, which is required for the error counter gate array (IC 17). This 2 x 24-bit counter is controlled by the 10 Hz clock and allows interrupt-free counting.

Description of c):

The clock module (IC 15) retains the date and time by means of built-in storage batteries in the instrument, even when the instrument is switched off. IC 16 is required as a bidirectional bus driver.

IC 9 acts as an interrupt expansion; the 10 Hz clock and "Peak rectifier overloaded" are reported.

9.2.10 RF CONTROL (G) [14/2019-F]

The following functions are implemented on the RF control:

- Current source DAC for sawtooth phase meter
- Lock-in DAC for 11 MHz loop
- Equalizer DAC for input circuit
- Lock-in FF for 11 MHz circuit lock-in monitoring
- Equalizer amplifier for the 0.2 - 1 kHz demodulator output
- Address decoding and control signal generation for:
  Controller 1
  Controller 2
  Input circuit
  Lock-in oscillator
  Carrier phase meter
- Operating voltage generators:
  +10 V for 11 MHz VCO
  -5.2 V stabilization

Current source DAC for sawtooth phase meter

The 12-bit DAC IC 11 generates a bit rate-proportional control voltage.
The reference element Gl 2 reduces the internally generated reference voltage by 2 V to +8 V.
The voltage-controlled current source following the DAC consists of IC 10 and T 3.
P 2 sets the steepness of the I/U characteristic, P 1 the zero point.

A negative potential is required at output Pt. 32 so that the set charging current can flow. The current mirror connected in the sawtooth phase meter fulfils this condition.

Lock-in DAC for 11 MHz loop

The lock-in DAC consists of the 8-bit DAC IC 22.
The required reference voltage of +2 V is supplied by IC 14/1.
The unipolar DAC output voltage of 0 ... 2 V (at Pin 9/IC 14/3) is transformed to the range -7 V ... +7 V by IC 14/4 and is available at 14 Pt. 40 as U_{lock} for controlling Controller 1 (9).

Equalizer DAC for input circuit (2)

The DAC consists of IC 13 and IC 14/2.
The output voltage can be set from 0 ... +2 V.

Lock-in FF

The lock-in FF IC 7/1 is set by the unlock pulses which are output by the lock-in detector in Controller 2 (7) when the 11 MHz circuit is unlocked. The FF can be polled via Tri-State buffer IC 8/1 and reset via the AAH address line.

Equalizer amplifier

The jitter demodulator has a lower limit frequency of approx. 2 Hz. So that lower jitter frequencies can also be evaluated, this drop in gain is compensated for in the equalizer amplifier.

Buffer stage IC 20 is followed by the actual equalizer, comprising IC 21/1 and IC 21/2.
A demod. signal equalized in the range 0.2 Hz - 1 Hz is available at output 14 Pt. 5.

10 V stabilization for 11 MHz VCO

The operating voltage of the 11 MHz VCO must be extremely free of interference. Consequently, a stabilizer circuit with high interference voltage suppression and correspondingly low noise is provided.

The 1.2 V reference voltage is supplied by the reference element IC 16 via the filter network R 36/C 22 to the controller comprising IC 23 and T 1. In order to increase the interference voltage suppression, the reference element is only fed with the start-up voltage via R 35 from +12 V. After settling, the voltage is supplied via R 37 from the stabilized +10 V voltage.

-5.2 V controller

This control circuit supplies the -5.2 V voltage supply for the RF section.
The reference voltage is supplied by the Zener diode Gl 1, which is supplied from the current source circuit with T 6. P 3 can be used to set the required voltage.

9.2.11 DISPLAY/CONTROL SECTION (L)

9.2.11.1 Display

The display consists of the 3 boards
- [2019-B] Display control
- [2019-C] Display
- [2019-X] Luminous field

Display control board [2019-B]

The display control consists of the assemblies
- Control processor + ROM + RAM
- Display driver
- Character generator
- Interface to I/O data bus of CPU-2A with interrupt logic
- Latches and drivers for luminous field
- 40 V voltage generator for vacuum fluorescence display with 7.8 V_{rms} heating voltage and +9 V cathode bias voltage

Control processor + ROM + RAM

The control processor used is an 80C31 microprocessor with
32 k x 8 external EPROM 27C256 and
8 k x 8 external RAM 6264.
In addition, IC 14 is required as an address latch.

This processor core can be switched to free-running via switches S 2/1 to S 2/6:

	S 2/1	S 2/2	S 2/3	S 2/4	S 2/5	S 2/6
Normal mode	on	off	on	off	on	off
Free-running	off	on	off	on	off	on
	= D3 = High		= D4 = Low		= D7 = Low	

ØØ ... ØF	INC reg.	1-byte commands
20 ... 2F	ADD A, reg.	
40 ... 4F	ORL A, reg.	
60 ... 6F	XRL A, reg.	

The clock frequency of the processor is 12 MHz. The command execution time in free-running mode is approx. 1 µsec, the frequencies on the address lines thus being
ARØ ... 1 MHz
AR1 ... 0.5 MHz

AR14 ... 61.03 Hz

For recording the signature, the signal ALE is used as clock and the signal A 15 as frame code (Start/Stop).

Note on signature analysis:
Since the 80C31 processor clocks the signal ALE (Adress Latch Enable) twice in each command cycle, the frame signature for the EPROM 27C256 has the value ØØØ1. This fact is already taken into account for the individual signatures in the signature list.

Display drivers

The display drivers form the interface between the logic signals from the processor and the character generator and the control signals for the display tube, which are switched between 0 V and 40 V.

- IC 19 and IC 25 are the column drivers for the grids of the display tube. The processor cyclically writes one "1" bit into the data input Pin (39) of IC 19, followed by 30 "0" bits. This means that only one display segment is switched on each time. The shift frequency (= multiplexer frequency) is approx. 2.9 kHz. Thus, the time for a complete writing cycle at 2.9 kHz is: 40 = 72.5 H. This avoids interference with lighting (neon lamps).
- IC 20 to IC 24 are the anode drivers; they are designed as Serial-In/Parallel-Out 12-bit registers. Each time the display is blanked via the strobe signal at the display drivers, the shift registers are loaded with the character to be displayed via the character generator with 12 clock pulses.

Character generator

The character generator comprises the decoding logic IC 9/4, IC 11/3/4/5 and IC 16/3, counter IC 17, latch IC 18, as well as the tables in EPROM IC 15 and the driver software.

To display a character, the processor reads the corresponding table from the EPROM. All these tables are at memory addresses > 7000 H. This memory access is detected by the decoding logic and the data read by the processor are simultaneously transferred into latch IC 18. Similarly, counter IC 17 is started. After three further processor command cycles, the latch contents are written into display drivers IC 20 to IC 24. This delay is necessary, as the display drivers have a setup time of 250 µsec.

After 12 processor read operations, the anode drivers are loaded with the bit pattern for character representation. This procedure is selected for reasons of time, in order to ensure an adequately high multiplexing frequency.

Interface to I/O data bus of CPU-2A and interrupt logic

The connection to CPU-2A is made via a 26-pin connector with the following pin assignments:

Pin 1	Ground	Pin 14	IO D5
2	-12 V	15	IO D4
3	IO AØ	16	IO D3
4	IO A1	17	IO D2
5	Reset	18	IO D1
6	IO A2	19	1ØØØ
7	IO A3	20	$\overline{\text{LSS}}$
8	IO A4	21	$\overline{\text{RD}}$
9	IO A5	22	$\overline{\text{WR}}$
IO	IO A6	23	+12 V
11	IO A7	24	+5 V
12	IO D7	25	RST 5.5 (only when used in PF 8 with S 1 closed)
13	IO D6	26	Ground ⊥

These are the standard assignments for the keyboard connection.

The modules IC 2 and IC 3 decode the I/O addresses 60 H to 67 H. These addresses execute the following functions:

60 H : Reading the display status
61 H : Output of a control command to the display
62 H : Transfer of data (write and read)
63 H, 67 H : Driving of 6 individual LEDs (PF 8 only)
64 H - 66 H: Driving of the luminous fields

A command is output from CPU-2A to the display control in the following steps:
- CPU-2A executes an OUT command to address 61.
- The decoded address 61 is combined with the $\overline{WR}$ signal to transfer the signals present on the I/O data bus to transceiver IC 7.
- At the same time, status FF IC 10/2 is set and the interrupt INT 1 applied to processor IC 12.
- In the interrupt-handling routine, the processor executes a RAM read command on address 800H. By combining address A 11 via IC 11/2 and the RD signal of the processor, the contents of the transceiver are thus read into the processor.
- An output at P 1.0 resets the status FF.

Data can be transferred in both directions. The transmission direction depends on the most recently output command.

CPU-2A can poll 2 status bits via address 60 H. Bit DØ = HIGH corresponds to the "Display control busy" status. No further commands or data may be transferred during this time. Bit D1 = HIGH indicates faults in the display control.

Latches and drivers for luminous fields

The settings for the luminous fields are stored in latches IC 4, 5 and 6. Groups of 4 LEDs connected in series are fed with a current of 4.3 V/470 Ω = 9 mA via resistors R 15/R 16 and pnp transistors T 5 ..., when a LOW signal is present at the base of the corresponding transistor (negative logic!).

Latches IC 26 and IC 27 for driving individual LEDs on the luminous field are not fitted on the PJM-4 version.

40 V voltage generator

A voltage transformer with switching controller IC 1 is used to generate the 40 V cathode voltage and the heating voltage. The switching frequency is in the region of 120 kHz.

FETs T 1 and T 4 alternately switch one part winding on the primary side of Ü 1 between +12 V operating voltage and ground. On the secondary side, the anode voltage is obtained by full-wave rectificaion with Gl 3 and Gl 4 and filtering with C 8. The heating voltage has a value of 7.8 V_{rms}. The superimposed cathode bias voltage of +9 V is generated with a voltage divider comprising R 10 and Gl 2.

The output voltages are not controlled. While the heating current has an almost constant value of 100 mA_{rms}, the anode current fluctuates between 15 and 50 mA. These two requirements cannot be fulfilled by a controller. The necessary voltage stability is achieved by the low-impedance dimensions.

Display board [2019-C]

The display consists of the 40-digit, 5 x 12-dot matrix vacuum fluorescence display 40 SD 42 Z and the wiring to the display control via four 26-pin flexible connectors. The display tube has 104 connector pins:

Pin 1, 80 Heating voltage/cathode bias voltage
+9 V DC voltage with superimposed 7.8 V_{rms} AC voltage

Pin 4 ... 77 60 anode connections for dot matrix, grouped as follows:

Top view Top right

1.1 4 24/2	2.1 5 23/2	3.1 6 22/2	4.1 7 21/2	5.1 8 20/2
1.2 9 24/1	2.2 10 23/1	3.2 11 22/1	4.2 12 21/1	5.2 13 20/1
1.3 14 24/20 1.4 19 24/19	2.3 15 23/20 2.4 20 23/19	3.3 16 22/20 3.4 21 22/19	4.3 17 21/20 4.4 22 21/19	5.3 18 20/20 5.4 23 20/19
1.5 24 24/18	2.5 25 23/18	3.5 26 22/18	4.5 27 21/18	5.5 29 20/18
1.6 30 24/17	2.6 31 23/17	3.6 32 22/17	4.6 33 21/17	5.6 34 20/17
1.7 47 24/14	2.7 48 23/14	3.7 49 22/14	4.7 50 21/14	5.7 51 20/14
1.8 52 24/13	2.8 53 23/13	3.8 55 22/13	4.8 56 21/13	5.8 57 20/13
1.9 58 24/12	2.9 59 23/12	3.9 60 22/12	4.9 61 21/12	5.9 62 20/12
1.10 63 24/11	2.10 64 23/11	3.10 65 22/11	4.10 66 21/11	5.10 67 20/11
1.11 68 24/10	2.11 69 23/10	3.11 70 22/10	4.11 71 21/10	5.11 72 20/10
1.12 73 24/9	2.12 74 23/9	3.12 75 22/9	4.12 76 21/9	5.12 77 20/9

Meaning:
Driver IC/IC Pin
-> See Display control

Pin 78 Cursor anode

Pin 86 ... 158 40 grid connections for digits, grouped as follows:

Meaning: Connector pin designation
Driver IC/IC Pin
See Display control

Grid	Connector pin	Driver IC	Pin	Display digit
G 1	86	25	18	right (top view)
G 2	88	25	17	
G 3	90	25	14	
G 4	91	25	13	
G 5	93	25	12	
G 6	95	25	11	
G 7	97	25	10	
G 8	99	25	9	
G 9	101	19	3	
G 10	103	19	4	
G 11	104	19	5	
G 12	106	19	6	
G 13	108	19	7	
G 14	110	19	8	
G 15	112	19	9	
G 16	114	19	10	
G 17	116	19	11	
G 18	117	19	12	
G 19	119	19	13	
G 20	121	19	14	
G 21	123	19	15	
G 22	125	19	16	
G 23	127	19	17	
G 24	128	19	18	
G 25	130	19	23	
G 26	132	19	24	
G 27	134	19	25	
G 28	136	19	26	
G 29	138	19	27	
G 30	140	19	28	
G 31	141	19	29	
G 32	143	19	30	
G 33	145	19	31	
G 34	147	19	32	
G 35	149	19	33	
G 36	151	19	34	
G 37	153	19	35	
G 38	154	19	36	
G 39	156	19	37	
G 40	158	19	38	left

Luminous field board [2019-X]

The luminous field board contains 6 luminous fields with 8 CQV231 chip LEDs each. The chip LEDs are connected in series in groups of four and are fed by one current source.
The connection to the display control is made via two 14-pin flexible connectors which (seen from the component side) are plugged into the socket rows b 1 ... b 19 and c 1 ... c 19 on the display board, starting at the left.

9.2.11.2 Keyboard [16/2019-A]

Key matrix

The keys are arranged in a matrix. Under normal circumstances, all columns have LOW potential. When a key is pressed, the output of IC 9, Pin 13, is set to HIGH via the OR function, thus triggering an interrupt. The processor then consecutively switches each column to LOW with IC 7, loading the row information via IC 6. The key pressed can be determined from the column and row number, whereupon the corresponding operating program is called up.

Debouncing circuit

The debouncing circuit used here is a so-called adaptive debouncing circuit: the longer a key bounces, the longer the debouncing time becomes.

The clock generator with IC 8/5 and 8/6 supplies the clock signals for the debouncing counters IC 10/1 and 10/2.

The signal at output IC 9, Pin 13, indicates whether a key is pressed (HIGH = key pressed).

"No key pressed" state:

If no key is pressed, counter IC 10/1 is not reset (resetting takes place via IC 8/3 and 8/1) and counts up to a value of 8. Output Q 3 (Pin 14) goes HIGH and inhibits the clock input (Pin 9), so that the counting operation is stopped. The other counter is reset via IC 8/2.

"Key pressed" state:

When a key is pressed, IC 9 supplies a HIGH signal. Counter IC 10/2 starts to run, since it is no longer reset via IC 8/2. It is always reset whenever a bounce pulse occurs. This resetting is repeated until the key is free of bounce for approx. 22 ms. After this time, the counter has reached a reading of 8 (Q 3 = HIGH), thus triggering the following operations:

- The counting operation of counter IC 10/2 is stopped (Pin 1 = HIGH).
- IC 10/1 is reset via IC 8/3 and 8/1 (AND combination of IC 9, Pin 13, and IC 10/1, Pin 6).
- Due to IC 8/2 and IC 8/4, IC 10/2 can thus no longer be reset by further bounce pulses.
- IC 11 is set and an interrupt thus triggered on the processor.

This state remains stable until the key is released.

"Key released" state:

When a pressed key is released, output IC 9 goes LOW. IC 10/1 is no longer reset and starts to run. As soon as a bounce pulse occurs, the counter is temporarily reset. This resetting is repeated until the key has been free of bounce for approx. 22 ms and has thus certainly been opened. Counter IC 10/1 has then reached a content of 8 (Q = 3). The "No key pressed" state (see above) is thus reached and IC 10/2 is reset.

Key LEDs

All LEDs can be driven via output gates IC 4 and IC 5.

Tone generator

The tone generator comprises multivibrator IC 3/2 and 3/3, driver stages IC 3/1 and T 1, and the piezoelectric signal generator W 1.

The frequency-determining time constants C 2/R 7 and C 3/R 4 can be halved by connecting R 5 and R 6 in parallel to generate the higher signal tone (activation of IC 4, Q 1).
The "beep" tone is switched on and off via IC 4, Q 0.

Drive table:

Address	Date	Tone
3 C	00	OFF
3 C	01	ON
3 D	00	Low
3 D	01	High

9.2.12 POWER SUPPLY UNIT (N)

9.2.12.1 Functional description of the power supply unit

The block circuit diagram of the PJM-4 power supply unit is shown in Fig. 9.2-43.

The high-end voltage of +19 ... +40 V generated in the transformer unit feeds the DC/DC converters for +12 V, -12 V, -6.3 V, +5 V, connected via the wiring card, the control unit mounted on the rear of the wiring card and the charging circuit alongside the mains filter.

The -5.2 V linear controller is switched by the output of the -6.3 V DC/DC converter.

The control unit produces a frequency of 405 kHz as the synchronization frequency for the DC/DC converters, measures the high-end voltage and outputs a "data save" signal if it drops below 16.5 V (at a mains voltage of $\leq$ 180 V).

The charging circuit supplies the 8 - 10 mA charging current for the three storage batteries and switches the data-save voltage from +5 V to battery voltage if the high-end voltage drops below 17.5 V.

The wiring card passes the high-end voltage generated in the transformer unit to the DC/DC converters and their output voltage to output socket e, from which the PJM-4 instrument is supplied.

The data-save voltage and the data-save signal also pass via the wiring card.

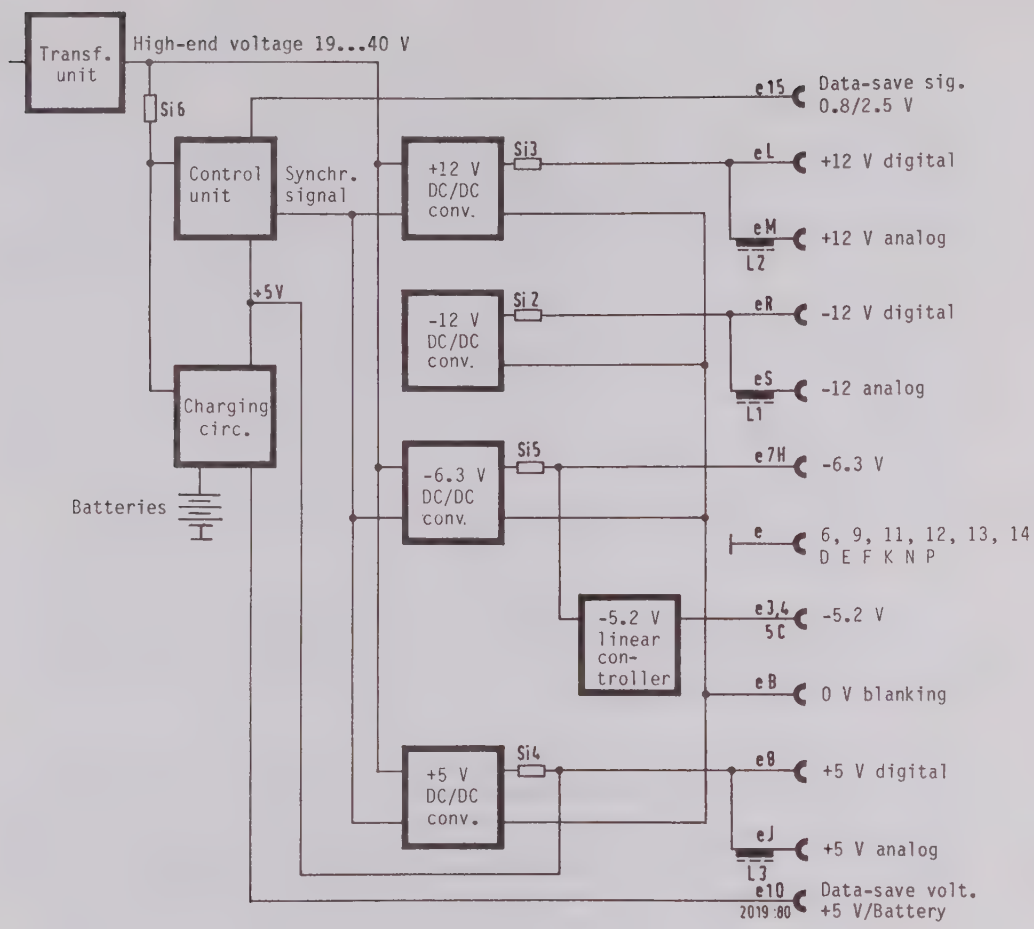


Fig. 9.2-43 Block circuit diagram, PJM-4 power supply unit

9.2.12.2 Circuitry description by functional groups

Transformer unit

The mains voltage arrives via the mains plug, mains filter, fuse Si 1 and mains voltage selector switch for 110/220 V at the transformer, whose secondary side feeds rectifier Gl 1. The latter supplies a high-end voltage of 19 ... 40 V (31 V at rated voltage and full load) at the charging capacitors.

Due to radio interference of the rectifier, an RC section is installed in parallel to the secondary winding of the transformer. It is located (from Series B onwards) on Charging circuit/ -5.2 V controller board [2019-AW].

Wiring card

The individual assemblies are mainly connected via the wiring card, which also accommodates all secondary fuses, the chokes for the filtered DC voltages (analog) and output socket e.

The charging circuit and the control unit have a common fuse Si 6. Otherwise, excessively high currents flow in the event of a short-circuit on one of the boards, thus destroying the conductors.

In order to avoid the need for special fire protection measures, the short-circuit current at the output of the DC/DC converters is limited to $\leq$ 8 A by fuses Si 2 ... 5.

Control unit

The data-save signal and the control voltage for the DC/DC converters are generated here. The control voltage consists of square-wave pulses of 5 - 6 V with a width of 200 ... 400 ns and a pulse repetition rate of 405 kHz ± 1 kHz.

The frequency-determining element is R 51, R 52 and C 13. The pulse height is determined by controller IC 11. The pulse repetition rate can be aligned with P 10.

The data-save signal is tapped at collector T 12. During normal operation ($U_{MAINS} \geq 180$ V), T 12 is open and current flows from U = +5 V via R 71, T 12, R 72, causing an output voltage of $\leq$ 0.8 V when fed with $\leq$ 10 mA.

If the mains voltage drops below 180 V (or the high-end voltage below 16.5 V), T 12 cuts off and a current of $\leq$ 0.3 mA can be tapped via R 71 at $\geq$ 2.5 V. The switching threshold can be set with P 11.

Charging circuit

The charging current supplies the charging current of 8 ... 10 mA for the storage batteries from the high-end voltage via T 1.
During this time, the +5 V voltage from the +5 V DC/DC converter is present at the output (socket 3 10) via T 2.
If the high-end voltage drops below 17.5 V, T 2 is cut off via IC 1 and the storage battery voltage is applied to the output (e 10) via Gl 1.
The switching threshold can be set with P 2.
In this case, the charging current from T 1 is cut off via diode threshold Gl 8.
If the high-end voltage rises again, T 2 is opened again, but with hysteresis via T 3 and T 4 only when this threshold adjustable with P 1 is exceeded.
The switching point is set to a high-end voltage of 19 V.
In Series A, the storage batteries are included on the board; from Series B onwards, they are installed separately from the power supply unit in the instrument.

-5.2 V linear controller

The -5.2 V linear controller is connected at the output of the 6.3 V DC/DC converter.
The -6.3 V, which is controlled anyway, is retained by reference diode Gl 15 and controlled via IC 5 and driver T 6 in power transistor T 7.
The voltage is set to 5.25 V with P 5.
Transistor T 7 is located on the side wall of the instrument for better cooling and is connected to the controller via the wiring card (Series B).
In Series A, the circuit is located on a small board on the rear of the wiring card.
From Series B onwards, it is mounted with the charging circuit alongside the mains filter.

DC/DC converters

Functional description of the converters:
The fundamental block circuit diagram of the DC/DC converter is shown in Fig. 9.2-44. At the same time, the blocks shown represent the boards in the converter.

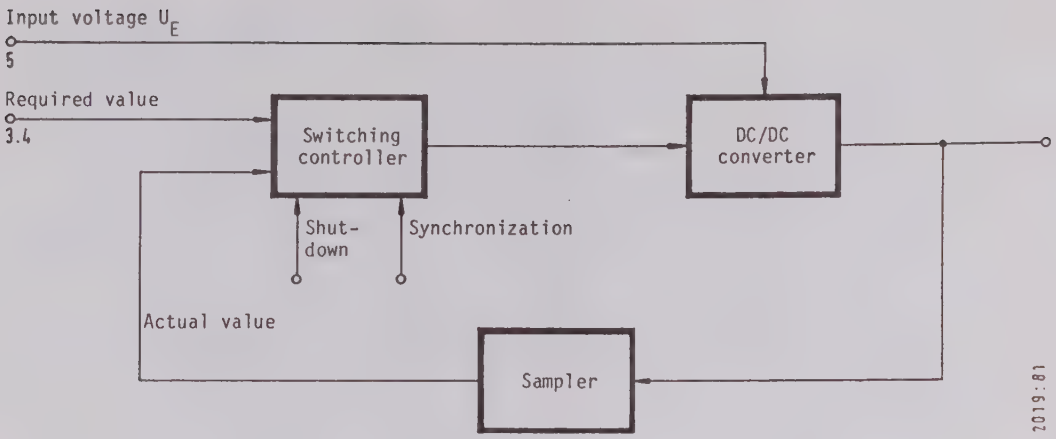
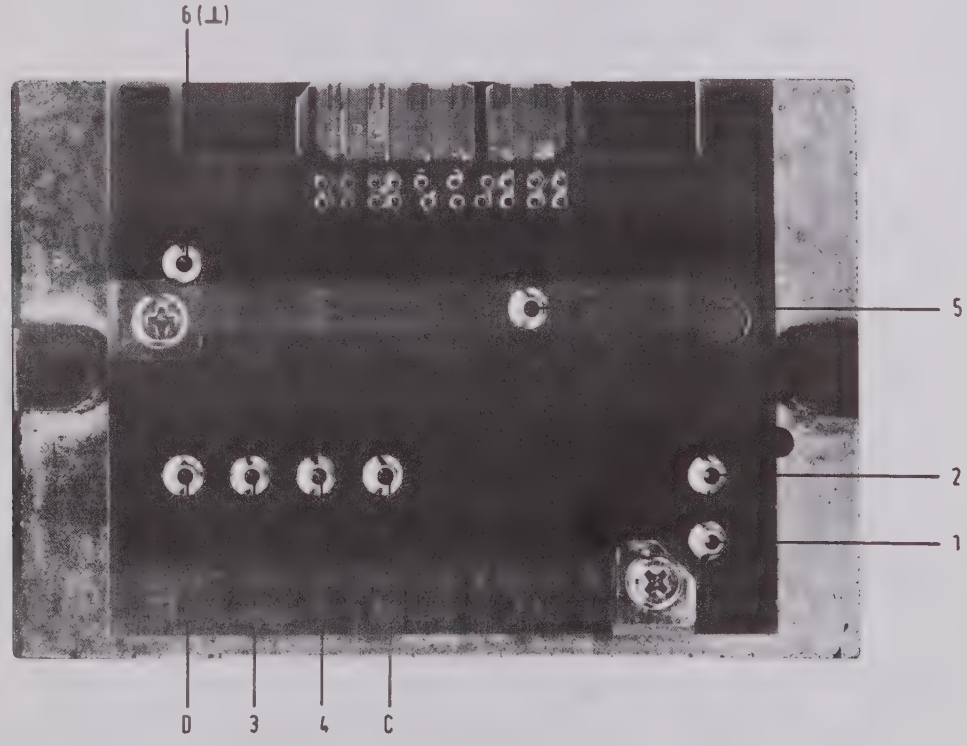


Fig. 9.2-44 Block circuit diagram of the DC/DC converter

For terminal assignments on the closed converter housing, see Fig. 9.2-45.



The required value of the output voltage is set on terminals 3 and 4 by means of a trimmer resistor or a fixed resistor.

The converter can be switched off via the Shut-Down input by applying +5 V. This input is at 0 V during normal operation.

Via the synchronization connection, the converter is operated in combination with other converters at a switching frequency defined by an external oscillator.

The output and input voltages of the converter are electrically isolated from each other.

Circuitry description of the converter assemblies:
The detailed block circuit diagram of the DC/DC converter module is shown in Fig. 9.2-46. The assignments to the individual assemblies are as follows:

DC/DC converter: Input filter
Control element
Output filter

Switching controller: Error amplifier
Pulse width modulator

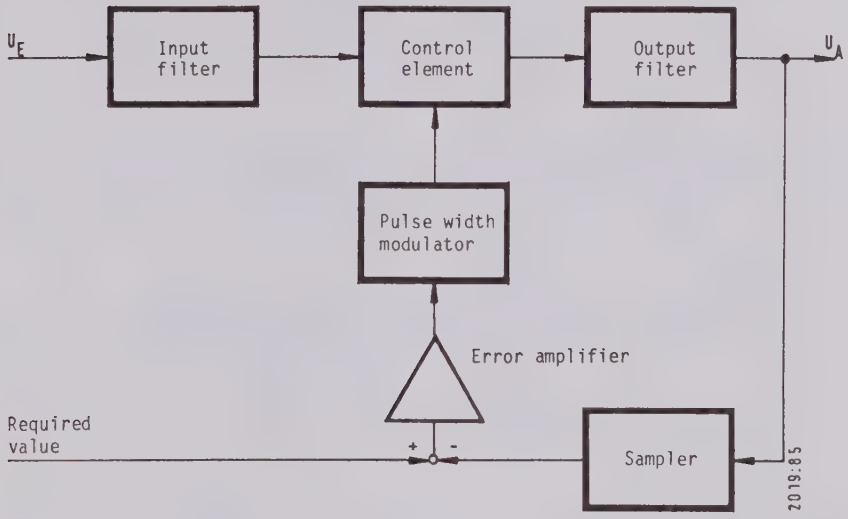


Fig. 9.2-46 Block circuit diagram

Input filter

The input filter is used to smooth the input current, thus minimizing the feedback of AC currents into the supply mains.

Control element

The control element consists of a push-pull power transformer, two power MOSFETs on the primary side and the double rectifier on the secondary side. In this unit, which operates as a push-pull forward converter, the DC voltage supplied from the input filter is chopped into two square-wave voltages with a frequency of ~ 200 kHz, offset by 180° in relation to each other, via the MOSFET switches. These voltages are transferred to the secondary side by the transformer and rectified into a square-wave voltage of f = 400 kHz by the double rectifier. The pulse duty factor of this square-wave voltage and thus the power transmitted on the secondary side, is controlled by the pulse width modulator.

Output filter

The rectified square-wave voltage of the control element is smoothed in the output filter. In addition, it is also ensured that the 400 kHz residual ripple is sufficiently filtered. The output variable of this unit is a DC voltage dependent on the pulse duty factor of the square-wave voltage.

Sampler

A voltage proportional to the output voltage is required to control the output voltage U_A. This electrically isolated voltage is transmitted to the primary side of the converter. A sample-and-hold element is used for this purpose. It transmits the output voltage to the primary side of the converter in a 400 kHz cycle by means of a transformer.

Error amplifier

The voltage supplied by the sampler is passed via additional filter and compensation elements to the error amplifier, where the actual and required output voltage values are compared.

Pulse width modulator

The pulse width modulator affects the pulse duty factor of the square-wave voltage in the control element as a function of the output voltage of the error amplifier. As the load decreases or the input voltage increases, the pulse duty factor is reduced to counter these disturbances. Conversely, the pulse duty factor is increased as the input voltage drops or the load increases. Thus, the output voltage is controlled.

Additional functions

In addition to the functions described so far, the converters also include a short-circuit-current limiter. The following versions are used, depending on Series:

- Short-circuit-current limiter

  In the case of output currents exceeding the rated converter current, the output voltage is reduced in accordance with the level of overloading. This version is not permanently short-circuit-proof.

- Version with fuse

  In this version, a picofuse is soldered into the connection between control element and output filter on the DC/DC converter board. It must be replaced when the maximum rated converter current has been exceeded.

9.2.13 DESCRIPTION OF THE PROCESSOR CARD CPU-2, BN 965, CIRCUIT DIAGRAM (90)

9.2.13.1 Reset and Mains OFF function

When the 5 V supply voltage is switched on, the processor is reset during the charging of R 7/C 4 via the CMOS gates (IC 4). In addition, the reset status is also forced for as long as the data-save input C 18 is not LOW. This data-save signal is usually generated by a so-called data-save circuit of the power supply unit. If it is LOW, i.e. if the operating voltage has reached its set-point value, the system must wait for C 3 to be charged. It then starts to run once the output of IC 4.6 ($\overline{\text{RESET IN}}$) goes HIGH.

If the processor writes into address 4, it resets the FF IC 3/1 (Q1) and thus itself forces a reset. This status is stable as long as the data-save input remains HIGH (even if the 5 V supply decreases).
FF IC 3 Q4 allows the data-save signal to be switched through to the TRAP interrupt.

Figure 9.2.13-1 shows the timing sequence of $\overline{\text{RESET IN}}$ during the power-up and power-down phases. For further details of the data-save function, also refer to Section 9.2.13.5.

In order to ensure a correct system reset in the event of only brief power-downs, capacitor C 3 is rapidly discharged via diode Gl 1 in the event of a self-reset, so that the full time constant of R 6/C 3 is always available at power-up.

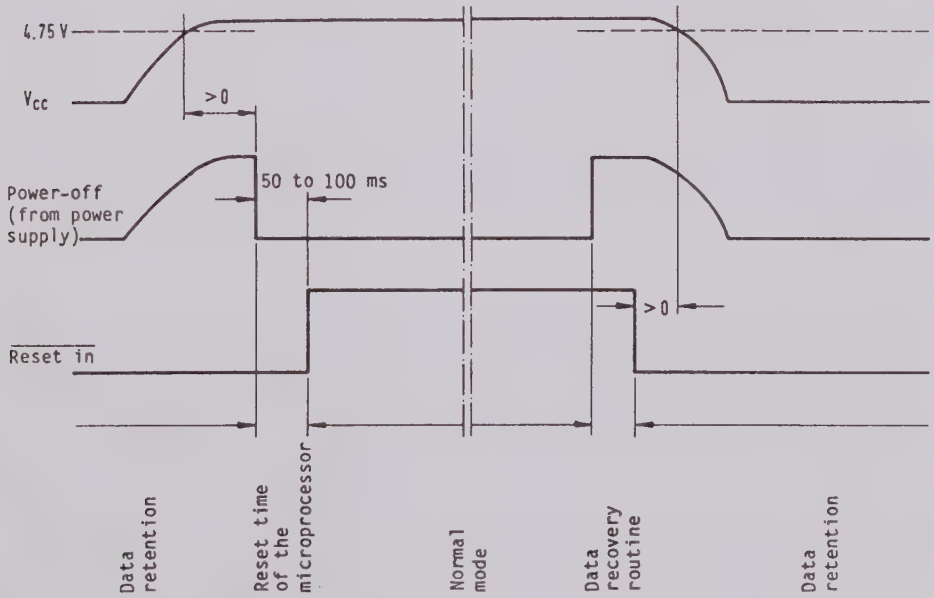


Fig. 9.2-47 Reset function following a data-save signal

9.2.13.2 Clock generation

The 8085 processor has an on-chip clock oscillator which operates with an 8 MHz crystal between Pin IC 41.1 and .2. The 4 MHz clock signal is available at Pin IC 41.37.

9.2.13.3 Latches, drivers and memories

The latch IC 40 receives the addresses from the multiplex bus ADØ-7 of the processor, so that the full address and data bus is available in parallel form. This latch is loaded by the trailing edge of ALE. The address and data buses are wired to the multi-point connector for DMA applications or memory expansions.

In order to split up the load on the buses resulting from the memories, the ROM and RAM buses are separate and connected to the processor via drivers IC 30 ... 33 and IC 34, 37.
The separate buffering of the RAM is also partly to do with the data-save function (see 9.2.13.5).

During troubleshooting, it must be remembered that the RAM address drivers IC 30 and IC 31 are inverters.

The strobe signals $\overline{RD}$ (= $\overline{OE}$) and WR are also buffered by driver IC 32.

Memory selection takes place via the demultiplexers IC 35 and 1/2 IC 36, which also disable the memories for I/O operations or external $\overline{DISMEM}$. The associated bus drivers are also involved in the memory select/deselect operation via corresponding control lines.

The select lines of the RAMs are wired via the analog switches in IC 25 which are closed during normal operation (see 9.2.13.5).

9.2.13.4 Control lines

$\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$:

In normal operation, the processor controls data transfer via these three control lines and the address and data buses. They are provided with pull-up resistors, so that no unintentional read or write pulses can occur in the reset or hold state. $\overline{RD}$, $\overline{WR}$ and IO/$\overline{M}$ can be operated externally in the hold state.

HOLD, HOLDA:

HIGH at the HOLD input causes the processor to switch to high impedance at the address and data buses, as well as at the control lines $\overline{RD}$, $\overline{WR}$ and IO/$\overline{M}$. It indicates this state by a HIGH signal at the HOLDA output. The processor resumes its program when HOLD returns to LOW. The LOW address latch IC 40 is switched to high impedance by HOLDA in parallel with the processor. The card is thus DMA-compatible. HOLD is a high-impedance input which must be activated for all events.

READY:

LOW at this input delays termination of the current read/write operation of the processor until it returns to HIGH. It allows adaptation to slow memories or peripherals. The I/O bus speed reduction circuit and the arithmetic processor (AP), both of which are on the card, use the Ready signal to stop the processor until they have completed their operations. Ready thus has a pull-up resistor R 10 and is connected to IC 11 via an open-collector gate and to the bus speed reduction circuit and AP by a wired-AND (see also 9.2.13.9 and 9.2.13.6). Additional speed reduction is possible via open-collector circuits connected via the multiway plug.

SO, S1, ALE, RST 7.5, RST 6.5, RST 5.5, SID, SOD:

These control lines and inputs/outputs are all wired out on the multi-point connector and, except for ALE, are only connected to the processor IC 41. Refer to the INTEL Data Book for their functions. The interrupt input INTR is not available and is connected to earth.

$\overline{\text{CLEAR}}$:

A negative edge at this card input generates a TRAP interrupt via NAND gate IC 5/2. This $\overline{\text{CLEAR}}$ edge can only arrive if the data-save input is LOW or the inhibit flip-flop IC 3/4 (Q 3) is HIGH. The user must ensure that the TRAP is enabled by setting the inhibit flip-flop IC 3/4 (Q 4 = HIGH) or by LOW at the data-save input in the event of interrupt requests by $\overline{\text{CLEAR}}$.

Independently, the LOW edge at $\overline{\text{CLEAR}}$ sets the flip-flop IC 3/3 (Q 2), which can be read in via the I/O switch IC 44. This possibility has been provided so that the program can establish whether a TRAP was triggered by the $\overline{\text{CLEAR}}$ input or the data-save input. This so-called $\overline{\text{CLEAR}}$ flip-flop is reset by writing into address 5 via demultiplexer IC 2. The AP is reset at the same time (see 9.2.13.6).

A number of card-internal control lines are described below:

RWIO:

RWIO goes HIGH for read or write operations in the I/O area.

$\overline{\text{ERAM}}$:

$\overline{\text{ERAM}}$ (Enable RAM) selects the highest 8 K of the address area intended for the RAM/AP.

$\overline{\text{ER3}}$:

$\overline{\text{ER3}}$ (Enable RAM 3) is the chip select for RAM 3. If card input C 19 is HIGH, no arithmetic processor, the top 1/2 K addresses of RAM 3 are suppressed and made available to the AP. In this case, $\overline{\text{ER3}}$ is HIGH from FEØØH to FFFFH.

WRRD:

This line (write or read) is the NAND circuit of the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ strobe. It is HIGH for every read or write operation.

9.2.13.5 Data-save

In the inactive state, CMOS RAM modules allow data to be retained with little power consumption. Therefore, their supply voltages are combined separately in U_{Bat} and wired out for connection to a battery.

Fig. 9.2-48 Connection of U_{Bat} to 5 V supply

When switched on, rectifier G1 6 supplies the RAMs from the 5 V source and tricklecharges a rechargeable battery.

Transition from normal to data-save mode:

A few milliseconds before the operating voltage drops below the low threshold, the power supply emits the "NETZ AUS" (Mains OFF) signal as a warning. If it is connected through to the TRAP, it triggers a non-maskable interrupt. The time remaining gives the processor the chance to store important data in the non-volatile RAM. It subsequently sets a flip-flop, whose output sets the $\overline{\text{RESET IN}}$ signal to LOW (see 9.2.13.1). This causes the analog switch IC 25 to open, thus pulling the chip select inputs of the RAMs to U_{Bat} by means of pull-up resistors R 17-20:

The RAMs are protected and no leakage current can flow via the chip select inputs into the remaining circuitry. If the 5 V supply voltage then disappears completely, all inputs/outputs of the RAMs are pulled to earth by pull-up resistors, this minimizing power consumption. The RAM area is buffered separately to prevent the pull-up resistors from burdening the rest of the system bus.

The FF generating the $\overline{\text{RESET IN}}$, IC 4/1 / IC 4/2, and the analog switch IC 25 are themselves connected to U_{Bat} and thus not affected by the drop in the 5 V supply. The inputs of this FF are also held close to 0 V by resistors.

Transition from data-save to normal mode:

Only when the operating voltage has reached its set-point value does the power supply give the enable signal by setting the data-save input to LOW. After expiry of the reset time R 6/C 3, the CMOS FF IC 4/1 / IC 4/2 can switch, this causing the LOW at $\overline{\text{RESET IN}}$ to disappear. The processor starts to run and the analog switch connects the RAM chip selects through. Refer to 9.2.13.1 for the timing of this sequence.

Checking the battery status:

Capacitor C 2 is connected to U_{Bat} via R 3, following this voltage with the relatively long time constant of

R 3 x C 2 = approx. 8 sec.

Shortly after switching on, a check can be made whether the battery voltage U_{Bat} was above the limit value of 3.2 V. Comparator IC 1 compares U_{Bat} at C 2 with the reference voltage formed from 5 V by R_1/R_2.

When the I/O switch has been switched over (UPW at LOW after writing to address 6), the comparator output IC 1.7 can be read into bit Ø of the I/O data bus.

This allows the processor to check the device to establish whether the battery voltage was still sufficient for data retention just before switching on.

9.2.13.6 Demultiplexer IC 2

Five $\overline{\text{RS}}$ FFs (IC 3/1 ... 4 and IC 6/3-4) are used for controlling these card features; they can be toggled, among other things, by demultiplexer IC 2.

Demultiplexer IC 2 is activated by writing into the address area of ROM Ø; it toggles the FF selected by the address, since its enable inputs are connected to the $\overline{\text{ROM Ø}}$ select and the $\overline{\text{WR}}$ strobe. ROM Ø remains passive during write operations. It should be noted that the address inputs A, B and C are activated with the inverted RAM addresses $\overline{\text{AØ}}$, $\overline{\text{A1}}$ and $\overline{\text{A2}}$.

9.2.13.7 Free-running

The CPU board has a free-running switch (S 1/7 to S 1/10) for this purpose. If the settings of S 1/7 to S 1/10 are inverted, the processor addresses the entire memory area cyclically, incrementing the address by one each time after a RESET. In order to record ROM signatures, the associated ROM select (test point) must be used as the START/STOP signal. The use of the free-running switch, in conjunction with the pull-up resistors of the data bus and the RD2 signal via G1 2 to AD6, ensures that only a subset of the 8085 command set is executed.

Bit number :	7	6	5	4	3	2	1	Ø
Logic level :	H	L	X	X	X	X	X	H
Machine code:	1	Ø	X	X	X	X	X	1 = 81H..BFH

X = any, data line not disconnected.

Note: The free-running switch only affects data lines Ø, 6 and 7.

Fig. 9.2-49 Value of the data bits for free-running

The commands involved are one-byte commands for arithmetic or logic operations which increment the program counter reading by one and thus yield a "program" with consecutive memory addressing.

9.2.13.8 I/O bus

The 8085 processor has input/output commands for serving its own I/O data and address bus. This bus is generally used to control a device. In order to prevent these ramified lines from carrying too much interference into sensitive circuits, W&G uses a special bus concept with the following features:

- Easily damped CMOS drivers/receivers.
- The address bus always has a defined value, only switching when necessary.
- The processor card holds the data bus at the old value when no data transfer is in progress.
- Special strobe signals allow simple connection of address decoders and data latches/drivers as peripherals (see 9.2.13.9).
- READY' input for deceleration of I/O operations as desired (see 9.2.13.9).
- Deceleration of I/O operations by binary input via inputs B1-B3 within fixed limits (see 9.2.13.9).

The following additional possibilities have also been provided:

- The output data can be read back for diagnostic purposes, i.e. the processor can read the output data back in while the connected peripherals are de-activated by the control lines.
- For special purposes (e.g. servicing), the I/O read gate IC 44 and IC 45 can be switched over to read switches S 1/1 to S 1/6, the CLEAR flip-flop (see 9.2.13.4) and the RAM battery monitor (see 9.2.13.5).

The I/O addresses are taken from the system bus by the CMOS latch IC 39 and constantly output externally.

Output data are taken from the system bus by the CMOS latch IC 42 (if LSS is HIGH) and switched to the I/O data bus. This happens during both an OUT and IN operation of the processor. A port range disable ($\overline{\text{PORT DIS}}$) flip-flop with the complementary outputs PORT DIS and $\overline{\text{PORT DIS}}$ can be controlled via demultiplexer IC 2.

If the $\overline{\text{PORT DIS}}$ output is switched to LOW, the I/O data driver IC 42 is activated constantly, meaning that the data can be read by driver IC 42 during an I/O read operation for diagnostic purposes. The output enable input of IC 42 is pulled to active LOW via diode G1 4.
IC 11/4 is a gate with open-collector output.

Input data are passed to the system bus by latch IC 43 (if IO/$\overline{\text{M}}$ is HIGH and $\overline{\text{RD}}$ is LOW). This latch is loaded with the data of switch IC 44, IC 45 by the LSS (Low-Speed Strobe).

Switch IC 44, IC 45 is set by the flip-flop IC 3/1 (Q3), the flip-flop itself being set by demultiplexer IC 2.

9.2.13.9 I/O timing control

In order to prevent I/O bus conflicts in a device due to the delay of the address decoders, the card generates not only the I/O data bus and the I/O address bus, but also special strobe signals $\overline{\text{RD}}$', $\overline{\text{WR}}$' and $\overline{\text{LSS}}$'. $\overline{\text{LSS}}$ is combined with the other two strobe signals by a logic AND:

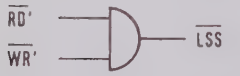


Fig. 9.2-50 Generation of the $\overline{\text{LSS}}$ signal

Each I/O operation consists of three time stages:

1. Addresses valid: Settling time for peripheral decoders
2. Strobe signal LOW: Data transfer ($\overline{\text{RD}}$ and $\overline{\text{WR}}$)
3. Waiting time: Resetting time for peripheral decoders

The three time stages can be varied (independently) via the three card inputs B 1-3. In positive logic, B 1-3 represents a 3-bit number:

$$n = < B\ 3, B\ 2, B\ 1 >,\ 0 \leq n \leq 7$$

This results in the following timing diagram for the I/O strobe signals and the I/O data- and address buses:

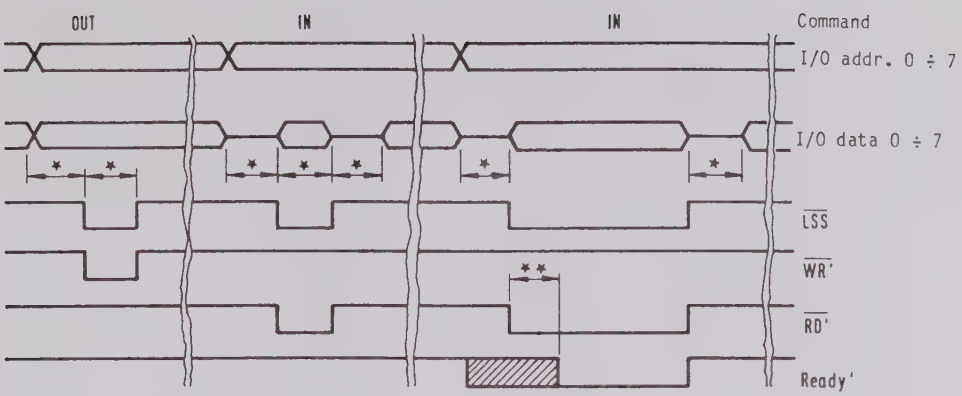


Fig. 9.2-51 IO timing

Stage 2 can be prolonged as desired by READY' = LOW.

Timing control sequence

The ALE signal resets the flip-flops IC 8/1, 8/2 and IC 9/2. Thus, as soon as an address for the I/O area is present on the data bus (IO/$\overline{M}$ = HIGH), the READY signal is switched to LOW via IC 10.8 and IC 11.4. Because the $\overline{Load}$ signal (IC 7.11) is LOW, counter IC 7 is already loaded with a value, e.g. ØAH (n = 5). READY also enables the clock for counter IC 7. As soon as the counter overflows, the next negative clock edge sets FF IC 8/2 (Q=H). IC 8/1 is connected downstream as a shift register cell, meaning that the counter receives a $\overline{Load}$ signal with the next-but-one clock edge.

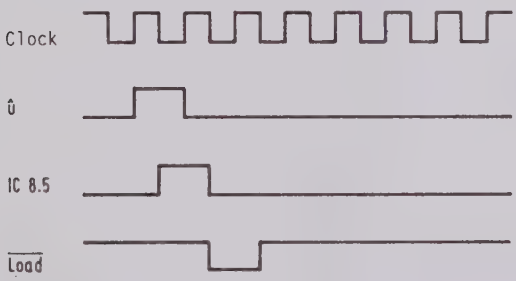
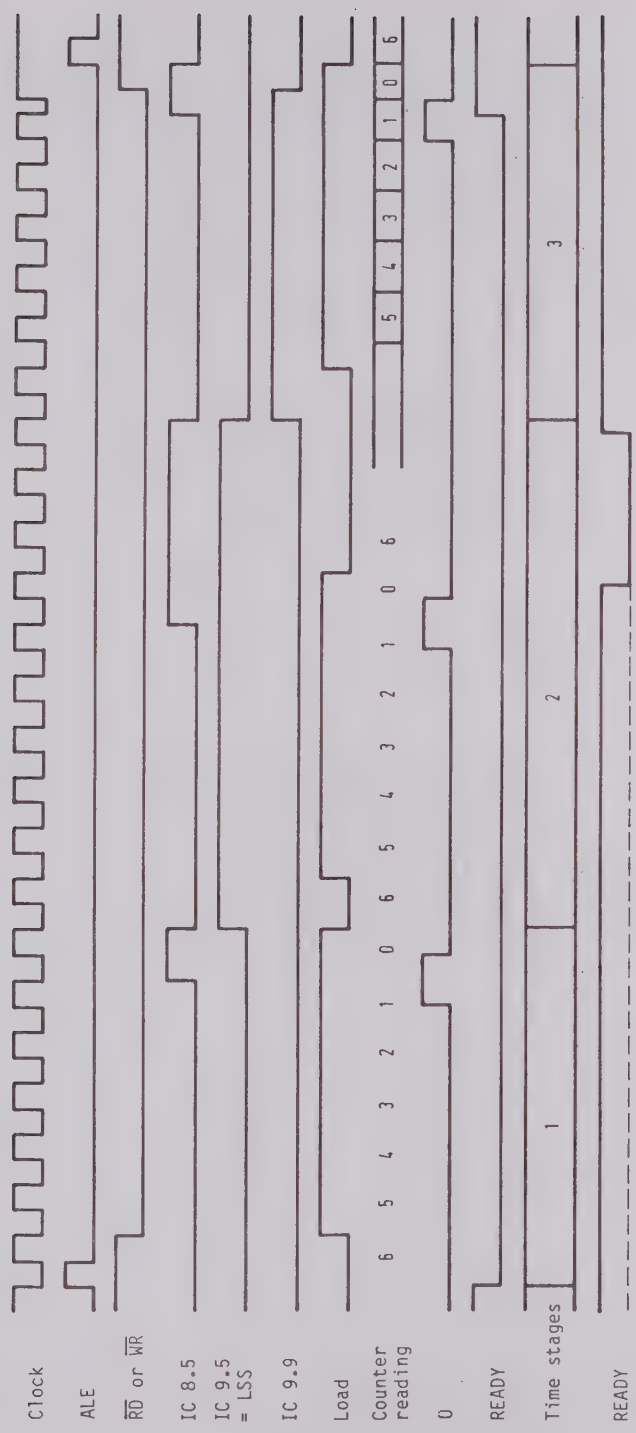


Fig. 9.2-52 Signal sequence for counter overflow

This procedure is repeated for each time stage.

At the end of the first time stage, i.e. when the counter first overflows, flip-flop IC 9/1 (Q = IC 9.5 = LSS) is set. When the counter overflows a second time, it is reset and FF IC 9/2 is set instead.

The third and final overflow then sets the READY signal to HIGH via IC 10.8 and IC 11.4 (waiting status cancelled) and the clock is inhibited. The decelerated procedure is terminated. The control signal RWIO present at IC 9.15 resets IC 9/1 and also has a safeguarding function: LSS pulses can only be generated when the processor needs to perform READ or WRITE operations.



Time stage 2 can be prolonged as desired with READY'. Counter IC 7 is loaded with the data B1-B3 at the start of each time stage.

Fig. 9.2-53 Timing control sequence - general situation

9.2.13.10 Test points

The card is provided with 2 x 8 test points:

Designation	Signal
OE	Output enable for ROMs, same as RD strobe
$\overline{ROM0}$	Not used for CPU-2A.
$\overline{ROM1}$	
$\overline{ROM2}$	
$\overline{ROM3}$	
$\overline{ROM4}$	For bank switching of ROMØØ to ROMØ4.
$\overline{ROM5}$	
$\overline{ROM6}$	
$\overline{RAM3}$	RAM 3 chip select
$\overline{RAM2}$	RAM 2 chip select
$\overline{RAM1}$	RAM 1 chip select
$\overline{RAM0}$	RAM Ø chip select
TP 4	$\overline{LSS}$ (Low-Speed Strobe)
TP 3	$\overline{WR}$' (Write strobe, I/O bus
TP 2	SOD (Serial Output Data from processor)
TP 1	$\overline{RD}$' (Read strobe, I/O bus)

Fig. 9.2-54 Test points

9.2.13.11 Bank switching

Bank switching occurs via ICs 50, 51 and 52. If output 6 of IC 50/3 is HIGH, IC1 is enabled and the selected EPROM is enabled.

9.2.14 IEEE 488 / <IEC 625> INTERFACE BUS CARD, BN 958, CIRCUIT DIAGRAM (91)

9.2.14.1 Functional description based on the block circuit diagram

Figure 9.2.14-1 is a simplified block circuit diagram of the <IEC 625> interface card.

The interface to the IEC bus with the necessary driver and receiver circuits is shown on the right-hand side.

The connection to the I/O bus of the device-internal microprocessor is shown on the other side.

For the microprocessor, the IEC bus interface represents a collection of input and output gates. It is via these gates that data are exchanged between the IEC bus and the device.

Data transfer between the IEC bus interface and the device is controlled by the IEC bus program. The PROMs in which this program is stored are located not on the IEC bus interface card, but in the device.

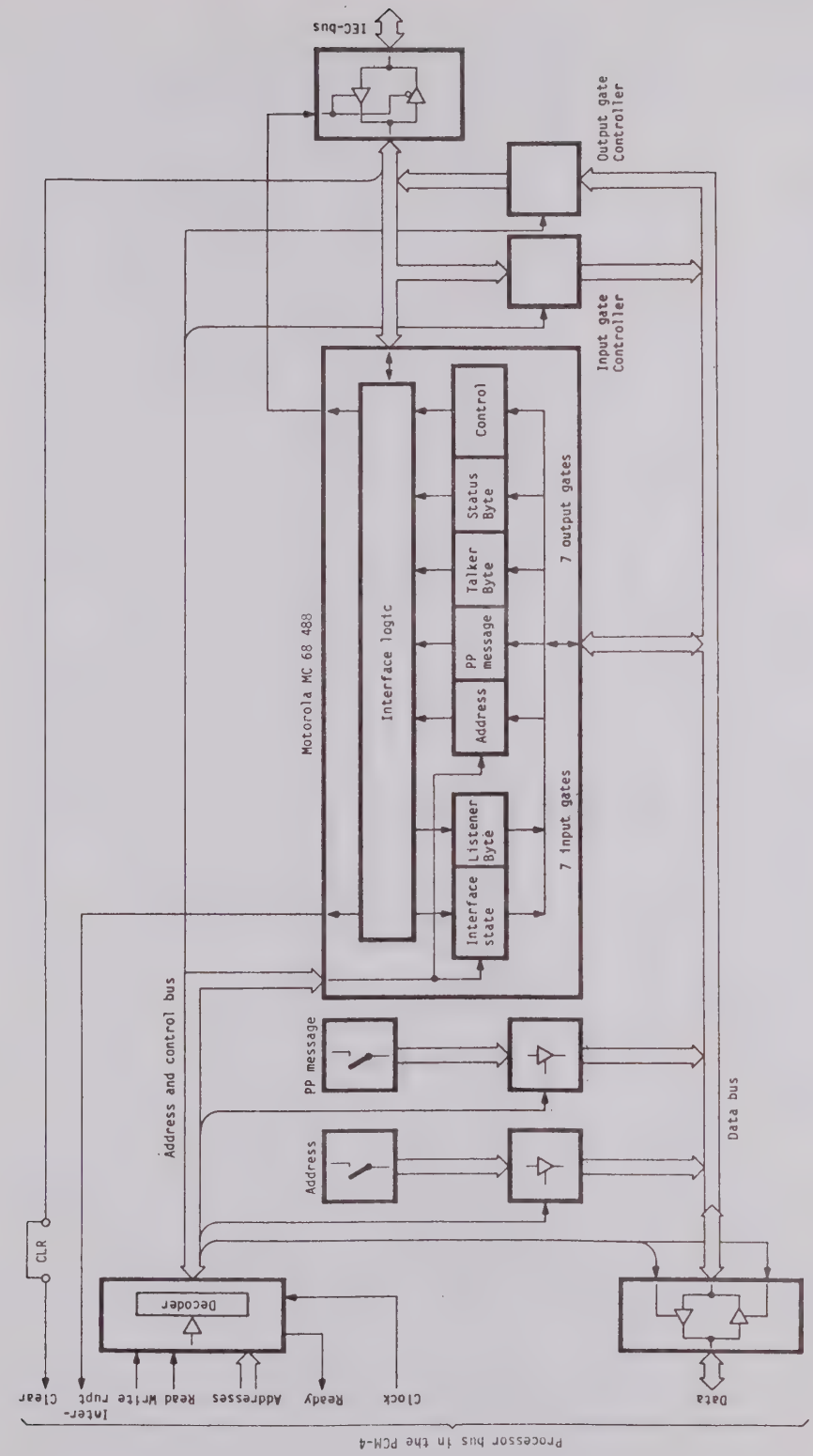


Fig. 9.2-55 Block circuit diagram of the IEEE 488/<IEC 625> interface bus card

9.2.14.2 Functional description of the card

The actual interface logic is located in the IEC bus interface module MC 68 488 from Motorola. This module handles the greater part of the interface tasks independently, i.e. without calling on the device-internal microprocessor. For example, it independently takes part in the IEC bus handshake cycle and decodes all messages transmitted on the IEC bus.

The interface states assumed on the basis of these messages are written into the corresponding input gates.

A further input gate acts as the transfer register for listener bytes. Listener bytes are the data transmitted from the IEC bus to the device while the device is addressed as listener, i.e. when setting parameters for the device are transmitted.

In addition to the input gates, the module also has output gates.

These are used

- to accommodate control commands which the microprocessor uses to influence the behaviour of the interface logic (e.g., among numerous other possibilities, it can stop the handshake cycle or send a Service Request SRQ via the IEC bus);
- as shift registers for bytes to be transmitted from the device to the IEC bus, e.g. talker bytes and status bytes. Talker bytes are the data transmitted from the device to the IEC bus while the device is operating as talker, e.g. when the measuring result is transmitted.

  The status byte is the devices response to a Serial Poll and contains the current device status.

  The "Address" switch is used for setting the device address.

  The "PP message" switch determines the IEC bus line on which the device is to transmit its Requested Service (RQS) status bit when the controller asks for its status by way of a Parallel Poll.

  In order to allow the BN 958 IEC bus interface to operate as the IEC bus controller the device -internal microprocessor must have direct access to certain IEC bus lines. This access is possible via the controller input gate and the controller output gate.

Interplay of device and IEC bus interface

When the IEC bus reaches a status requiring control by the device-internal microprocessor, the IEC bus interface sends an interrupt to the device. This interrupt then causes the microprocessor to execute the IEC bus program (see Fig. 9.2.14-2). This is the case if, for example,

- the device is to be switched from local to remote control or vice versa,
- a listener byte has been transmitted via the IEC bus. The interface logic has then written this byte into the transfer register for listener bytes and stopped the handshake cycle. The handshake cycle remains interrupted until the microprocessor reads this byte (whereupon the IEC bus line NDAC goes HIGH). Once the listener byte has been processed and stored, the IEC bus line NRFD also goes HIGH.

- the device must provide a new talker byte. When the new talker byte is written into the corresponding output gate, the handshake cycle is started by the IEC bus line DAV being switched to LOW.
- the device is to be triggered by the IEC bus command "Device Trigger (GET)" in order to perform a measurement. The interface logic has then stopped the handshake cycle. It remains interrupted until the microprocessor has started the measurement and then re-enables the handshake cycle (NDAC = HIGH and NRFD = HIGH).
- the device is to be set to a defined initial status by the IEC bus command "Device Clear (DCL or SDC)". Again, the interface logic will have stopped the handshake cycle. It remains interrupted until the microprocessor has set the device to the initial status and then re-enables the handshake cycle (NDAC = HIGH and NRFD = HIGH).

If the CLR jumper is fitted on the IEC bus or if switch S 3 is closed, the IEC bus signal IFC (Interface Clear) causes initialization of the device. In the event of an interlock condition, the device can always be initialized via the IEC bus. (This is important for devices in unmanned stations where an interlock condition caused by external disturbances cannot be eliminated by switching the mains power off and back on.)

9.2.14.3 Structure of the IEC bus program

(The program is implemented on the CPU board)

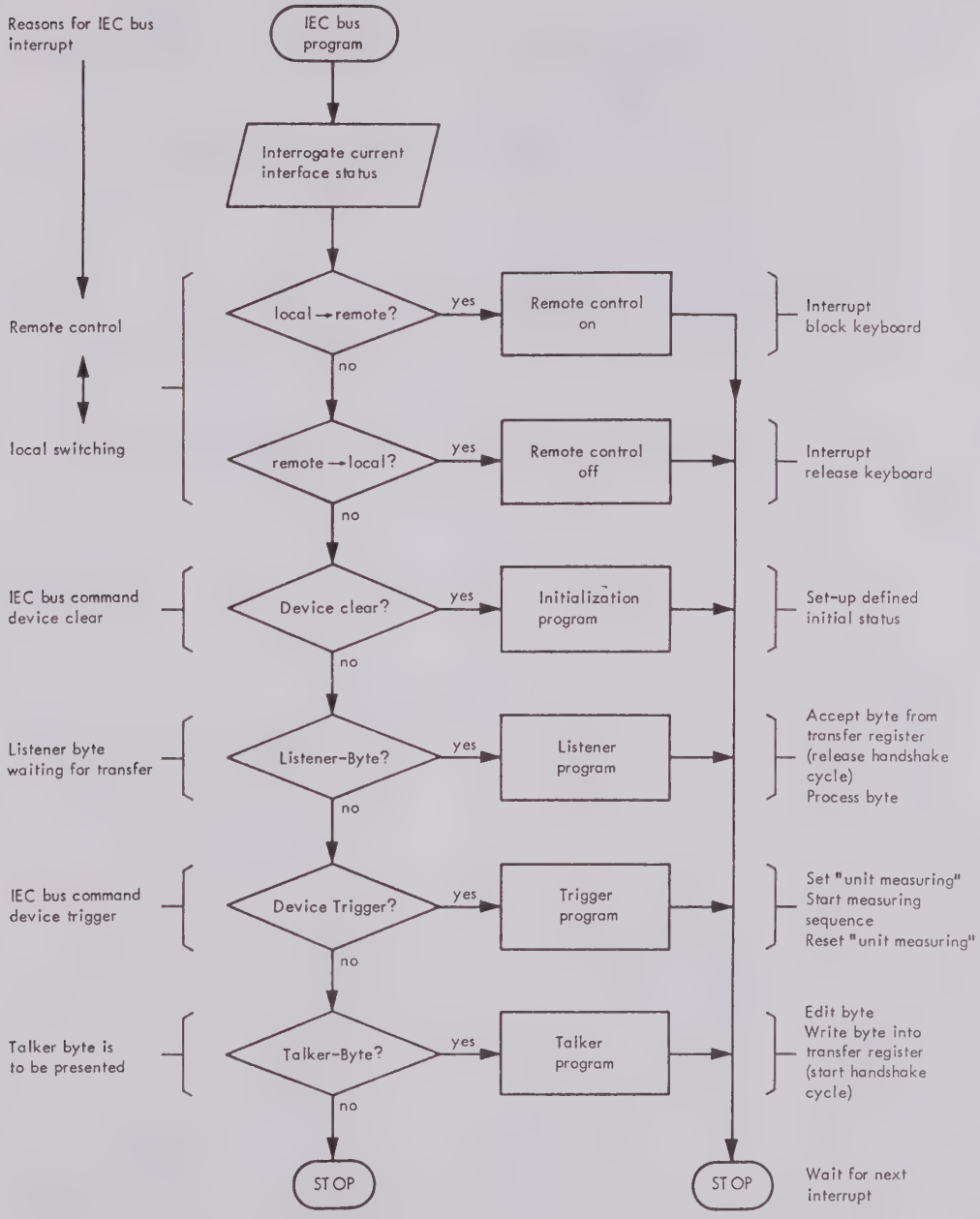


Fig. 9.2-56 Structure of the IEC bus program

9.3 SOFTWARE DESCRIPTION

The standard instrument software includes a number of menu-based support programs for test and service purposes:

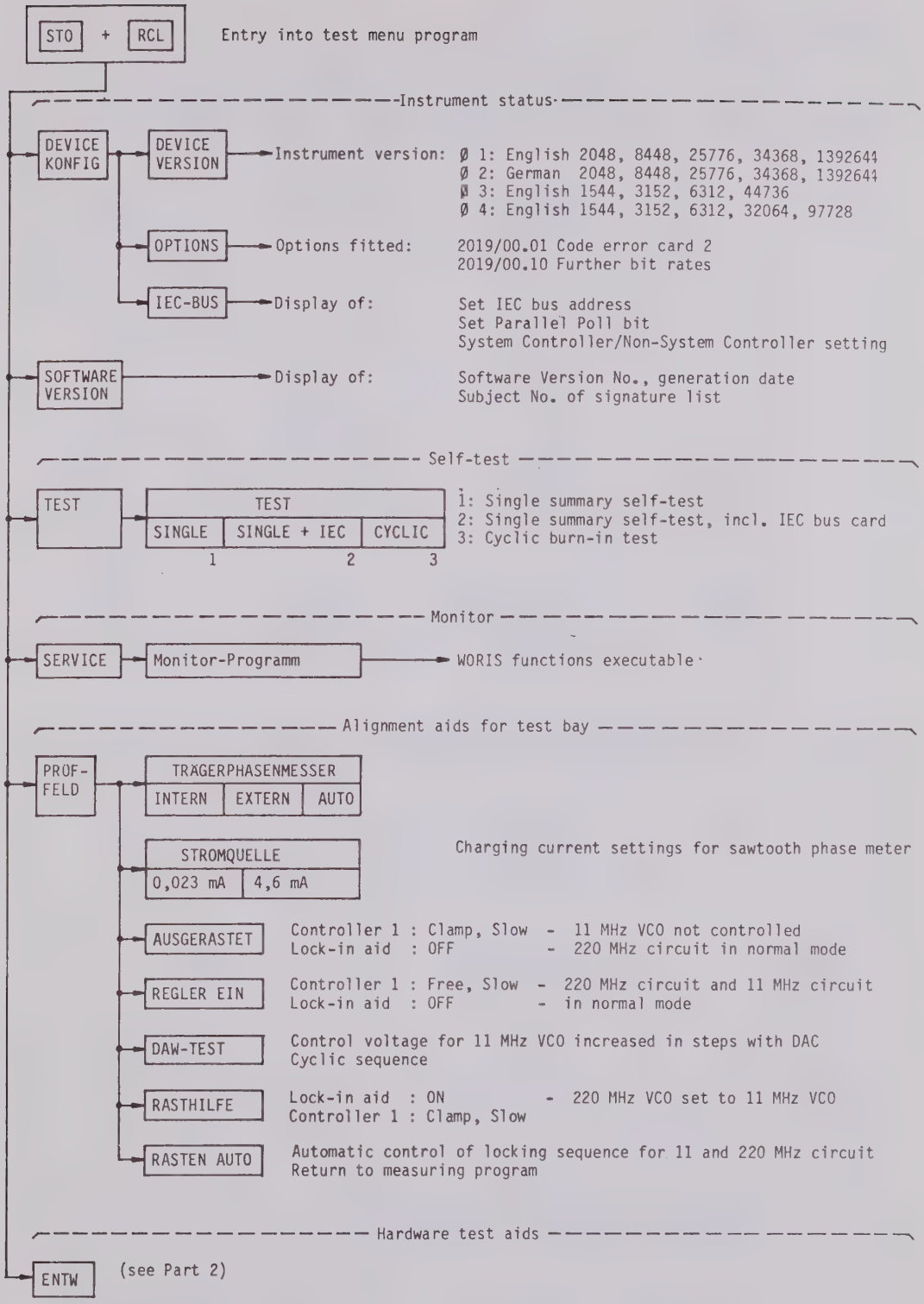
- Instrument version: "DEVICE KONFIG"
- Self-test program : "TEST"
- Monitor program : "SERVICE"
- Test menus : "PRUEFFELD" and "ENTW"

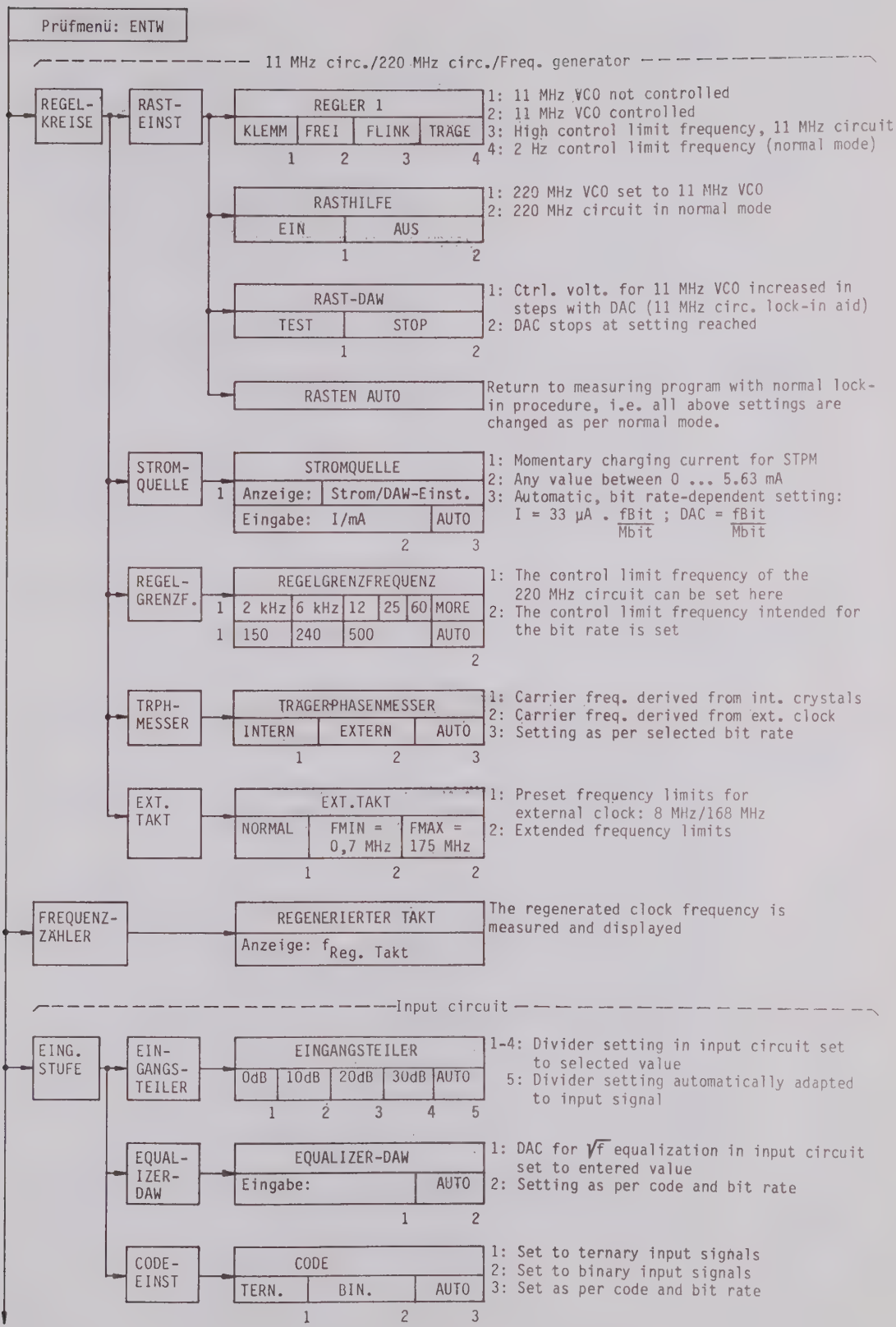
In addition to the self-test and monitor programs, the "ENTW" test menu is a particularly useful tool for service work.

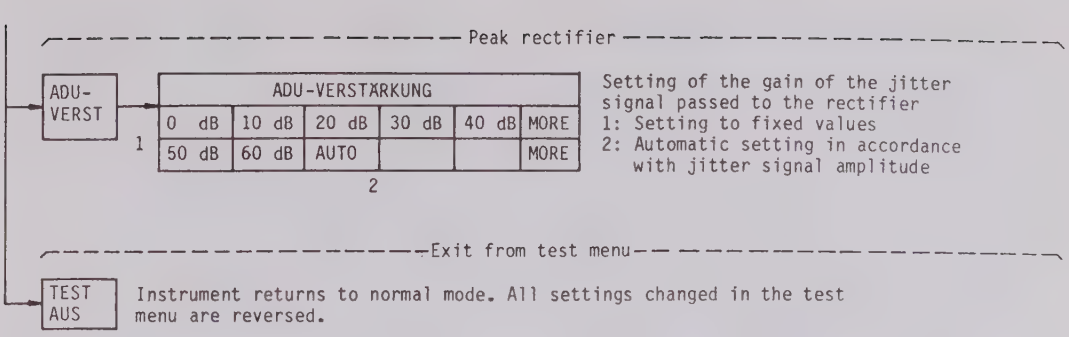
Calling up the support programs:

The support program menu is entered by simultaneously pressing STO and RCL.

The functions RETURN and CLR are also available when paging through these menus.


STO + RCL
Entry into test menu program
Instrument status
DEVICE KONFIG
DEVICE VERSION
Instrument version: Ø 1: English 2048, 8448, 25776, 34368, 1392644
Ø 2: German 2048, 8448, 25776, 34368, 1392644
Ø 3: English 1544, 3152, 6312, 44736
Ø 4: English 1544, 3152, 6312, 32064, 97728
OPTIONS
Options fitted: 2019/00.01 Code error card 2
2019/00.10 Further bit rates
IEC-BUS
Display of: Set IEC bus address
Set Parallel Poll bit
System Controller/Non-System Controller setting
SOFTWARE VERSION
Display of: Software Version No., generation date
Subject No. of signature list
Self-test
TEST
TEST
SINGLE
SINGLE + IEC
CYCLIC
1
2
3
1: Single summary self-test
2: Single summary self-test, incl. IEC bus card
3: Cyclic burn-in test
Monitor
SERVICE
Monitor-Programm
WORIS functions executable
Alignment aids for test bay
PRÜF-FELD
TRÄGERPHASENMESSER
INTERN
EXTERN
AUTO
STROMQUELLE
0,023 mA
4,6 mA
Charging current settings for sawtooth phase meter
AUSGERASTET
Controller 1 : Clamp, Slow - 11 MHz VCO not controlled
Lock-in aid : OFF - 220 MHz circuit in normal mode
REGLER EIN
Controller 1 : Free, Slow - 220 MHz circuit and 11 MHz circuit
Lock-in aid : OFF - in normal mode
DAW-TEST
Control voltage for 11 MHz VCO increased in steps with DAC
Cyclic sequence
RASTHILFE
Lock-in aid : ON - 220 MHz VCO set to 11 MHz VCO
Controller 1 : Clamp, Slow
RASTEN AUTO
Automatic control of locking sequence for 11 and 220 MHz circuit
Return to measuring program
Hardware test aids
ENTW
(see Part 2)


Prüfmenü: ENTW
11 MHz circ./220 MHz circ./Freq. generator
REGEL-KREISE
RAST-EINST
REGLER 1
KLEMM | FREI | FLINK | TRÄGE
1 2 3 4
1: 11 MHz VCO not controlled
2: 11 MHz VCO controlled
3: High control limit frequency, 11 MHz circuit
4: 2 Hz control limit frequency (normal mode)
RASTHILFE
EIN | AUS
1 2
1: 220 MHz VCO set to 11 MHz VCO
2: 220 MHz circuit in normal mode
RAST-DAW
TEST | STOP
1 2
1: Ctrl. volt. for 11 MHz VCO increased in steps with DAC (11 MHz circ. lock-in aid)
2: DAC stops at setting reached
RASTEN AUTO
Return to measuring program with normal lock-in procedure, i.e. all above settings are changed as per normal mode.
STROM-QUELLE
STROMQUELLE
1 Anzeige: | Strom/DAW-Einst.
Eingabe: I/mA | AUTO
2 3
1: Momentary charging current for STPM
2: Any value between 0 ... 5.63 mA
3: Automatic, bit rate-dependent setting:
I = 33 µA . fBit/Mbit ; DAC = fBit/Mbit
REGEL-GRENZF.
REGELGRENZFREQUENZ
1 2 kHz | 6 kHz | 12 | 25 | 60 | MORE
1 150 | 240 | 500 | AUTO
2
1: The control limit frequency of the 220 MHz circuit can be set here
2: The control limit frequency intended for the bit rate is set
TRPH-MESSER
TRÄGERPHASENMESSER
INTERN | EXTERN | AUTO
1 2 3
1: Carrier freq. derived from int. crystals
2: Carrier freq. derived from ext. clock
3: Setting as per selected bit rate
EXT. TAKT
EXT.TAKT
NORMAL | FMIN = 0,7 MHz | FMAX = 175 MHz
1 2 2
1: Preset frequency limits for external clock: 8 MHz/168 MHz
2: Extended frequency limits
FREQUENZ-ZÄHLER
REGENERIERTER TAKT
Anzeige: f Reg. Takt
The regenerated clock frequency is measured and displayed
Input circuit
EING. STUFE
EIN-GANGS-TEILER
EINGANGSTEILER
0dB | 10dB | 20dB | 30dB | AUTO
1 2 3 4 5
1-4: Divider setting in input circuit set to selected value
5: Divider setting automatically adapted to input signal
EQUAL-IZER-DAW
EQUALIZER-DAW
Eingabe: | AUTO
1 2
1: DAC for √f equalization in input circuit set to entered value
2: Setting as per code and bit rate
CODE-EINST
CODE
TERN. | BIN. | AUTO
1 2 3
1: Set to ternary input signals
2: Set to binary input signals
3: Set as per code and bit rate


Peak rectifier
ADU-
VERST
ADU-VERSTÄRKUNG
0 dB
10 dB
20 dB
30 dB
40 dB
MORE
50 dB
60 dB
AUTO
MORE
1
2
Setting of the gain of the jitter signal passed to the rectifier
1: Setting to fixed values
2: Automatic setting in accordance with jitter signal amplitude
Exit from test menu
TEST
AUS
Instrument returns to normal mode. All settings changed in the test menu are reversed.

9.3.2 DESCRIPTION OF "ENTW" TEST MENU

This test menu makes it possible to
- monitor,
- fix or
- set

almost all automatic hardware settings.

The test menu is largely self-explanatory and only offers those settings which the measuring software can in fact set.

Control of instrument behaviour:

The functions
- CLR : "Page up" in the menu and
- RETURN: Return to the measuring program

remain unaffected.

If an instrument setting is changed via the test menu and thus inaccessible to automatic setting, the instrument continues to operate with the new setting and all other automatic functions.

During troubleshooting, for example, this allows:
- testing of the instrument behaviour with fixed instrument settings,
- separate operation of sub-assemblies,

etc.

Return to measuring program:

Return with changed instrument setting:
Some setting menus (e.g. "input divider") include an automatic return to the measuring program. In all other menus, the return function is controlled by the RETURN key.

Return to normal AUTO mode of all instrument functions:
Three possibilities:
- Switch instrument OFF/ON, or
- Select "AUTO" function in all changed menu sections, or
- Select "TEST OFF" in the test menu.

Identification of changed hardware settings:

Since hardware settings which have been changed in the test menu and are thus not accessible to automatic adjustment can lead to faulty instrument behaviour, the word "TEST" is displayed in the measuring program in place of the COUNT. STATUS as a reminder.

Instrument error messages:

If a setting is withdrawn from automatic control, no error messages relating to the instrument function involved are generated.

E.g.: Changes in the "LOCK-IN SETTING" test menu suppress the "SYNC LOSS" message.

Specific suppression of error messages:

If an error message is to be suppressed, it will suffice to make a corresponding setting in the test menu, e.g. by manually specifying the AUTO setting indicated by the cursor.

E.g.: The "NO SIGNAL" message is to be suppressed because the input section is to be bypassed for operating the instrument:
-> Specify the setting in the "INPUT DIVIDER" menu.

Cursor:

The current instrument setting in automatic or manual mode is indicated by a cursor.

9.3.3 SELF-TEST MENU "TEST"

A choice can be made between three self-test versions:

"SINGLE":

Test sequence as for Mains ON: ROM test
RAM test
I/O test
Display test
Hardware (10 Hz clock, keyboard, real-time clock)

Error messages : See list in Section 4.2.2 -

"SINGLE + IEC":

Test sequence : As for "SINGLE" plus test of IEC bus card

Only to be used if IEC bus card fitted; otherwise error message.

"CYCLIC":

Test sequence : As for "SINGLE", but in endless loop for burn-in test (no IEC bus test!)

Exit : Only possible via Mains OFF/ON

9.3.4 MONITOR PROGRAM "SERVICE" (WORIS FUNCTIONS)

The key assignments of the PJM-4 after calling up the monitor program are shown in Fig. 9.3-1.

Refer to Section 2.3.4 for a description of the monitor functions.

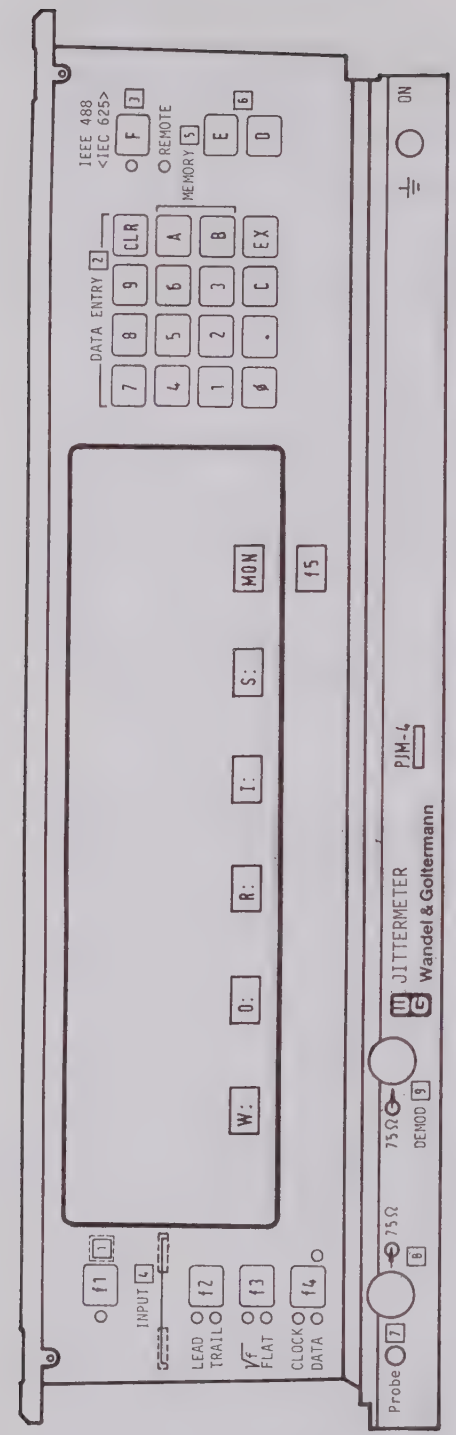


Fig. 9.3-1 Key assignments in "SERVICE" mode

9.3.5 CYCLIC HARDWARE REPAIR PROGRAMS

The repair programs can be called up via

- appropriate setting of DIP switches S 1 ... S 6 on CPU-2A
- the monitor command S: < address > [EX']

All repair programs run in an endless loop. They can only be exited by returning the DIP switches to the original settings and Mains OFF/ON.
The following individual programs are available:

- Cyclic address decoder test, range $A0_H$ ... AB_H

  The commands IN $A0_H$ ... IN AB_H are executed cyclically. This allows testing of the address decoding of the I/O bus via modules IC 1, IC 2 on the RF control (14) and the following modules by means of an oscilloscope or logic test probe.

- Cyclic address decoder test, range $B0_H$ ... BF_H

  See above; test for IC 4, IC 5, IC 6 on the RF control (14)

- Cyclic DAC test, sawtooth phase meter current source
  The output voltage V_{out} (Pin 9) of IC 11 is varied in sawtooth form between 0 V and +8 V.

- Cyclic DAC test, lock-in DAC
  The output voltage at IC 14/4, Pin 14, is varied in sawtooth form between -7 V and +7 V.

- Cyclic DAC test, equalizer DAC
  The output voltage at IC 14/2, Pin 7, is varied in sawtooth form between 0 V and +2 V.

- Cyclic address decoder test, range 80_H ... 97_H

  See above, test for IC 14 on the hit counter (13)

- Cyclic DAC test, threshold setting
  The voltage at TP 8 on the hit counter (13) is varied in sawtooth form between 0 V and +4.5 V

- Cyclic LED test
  All LEDs, luminous fields and the beep tone generator are switched on and off in the following order:

  LED LEAD
  LED TRAIL
  LED $\sqrt{f}$
  LED FLAT
  LED CLOCK
  LED DATA
  LED PANEL LOCK
  LED AIS
  LED LOCAL + High beep tone
  LED REMOTE + Low beep tone

Luminous field AVERAGE, right
Luminous field AVERAGE, left
Luminous field LOWPASS, right
Luminous field LOWPASS, left
Luminous field CODE, right
Luminous field CODE, left
Luminous field BITRATE, left
Luminous field BITRATE, right
Luminous field TIME, right
Luminous field TIME, left
Luminous field COUNT STATUS, right
Luminous field COUNT STATUS, left
Luminous field CODE ERROR, right
Luminous field CODE ERROR, left
Luminous field JITTER, left
Luminous field JITTER, right
Luminous field PHASEHITS, left
Luminous field PHASEHITS, right
Luminous field THRESHOLD, left
Luminous field THRESHOLD, right
Luminous field GATING, left
Luminous field GATING, right
Luminous field HIGHPASS, left
Luminous field HIGHPASS, right

- Cyclic keyboard test
  The key matrix is polled cyclically. Each key pressed is shown on the display.

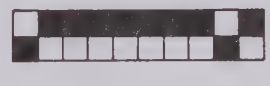
- Cyclic display test (data)
  Commands are cyclically output to the display controller to display all possible characters in upper and lower-case letters at top and bottom.

- Cyclic display test (commands)
  Control commands for the cursor are output cyclically. The cursor is switched on from right to left.

- Cyclic address decoder test, range $C0_H$ ... $E6_H$

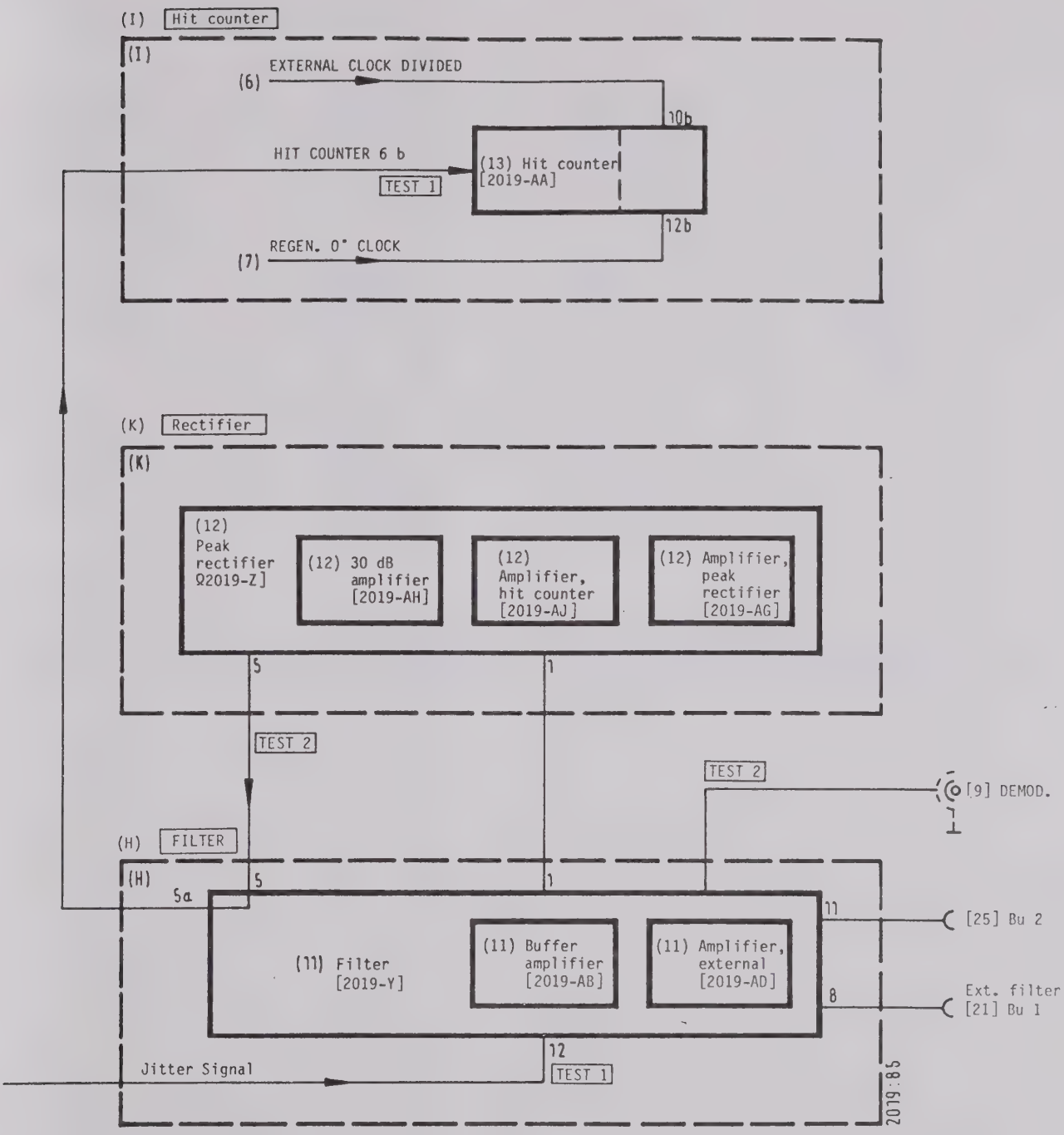
  See above; the decoder modules on the Filter (11), Peak rectifier (12) and Code error 1 (3) circuits are tested.

DIL switch coding and start addresses for the test programs

DIL switch code (CPU-II card) (black = pressed)	Start address for monitor command S: ...	Test program
		"Normal" switch setting
		"Monitor" mode
	ØDDH	Cyclic overall self-test
	ØE3H	Cyclic EPROM test
	ØE9H	Cyclic RAM test (non-destructive)
	ØEFH	Cyclic I/O test
	ØF5H	Cyclic test of the arithmetic processor not applicable
	ØFBH	Cyclic test of the screen control card not applicable
	101H	Cyclic test of the IEC bus interface
	107H	Cyclic RAM test (destructive)
	10DH	Cyclic address decoder test, range $A0_H$ ... AB_H (RF control)

	113H	Cyclic address decoder test, range $B0_H$ ... BF_H (RF control)
	119H	Cyclic DAC test, current source (RF control)
	11FH	Cyclic DAC test, Controller 1 locking (RF control)
	125H	Cyclic DAC test, equalizer (RF control)
	12BH	Cyclic address decoder test, range 80_H ... 97_H (hit counter)
	131H	Cyclic DAC test, hit threshold (hit counter)
	137H	Cyclic LED test (keyboard/display)
	13DH	Cyclic keyboard test
	143H	Cyclic display test (data)
	149H	Cyclic display test (commands)
	14FH	Cyclic address decoder test, range $C0_H$ ... $E6_H$
		Display "1005" for all other switch settings
		Free-running

10 BLOCK CIRCUIT DIAGRAMS..... 10-1



Circuit-related block circuit diagram

Wandel & Goltermann-Vertriebsstellen

Deutschland

Wandel & Goltermann
Vertriebsgesellschaft
Arbachtalstraße 6
Postfach 1262
7412 Eningen u.A.
Tel. (07121) 86 15 11
Telex 7 29 833 wug d
Fax (07121) 86 20 28

Wandel & Goltermann
Technisches Büro Berlin
Halemweg 17-19
1000 Berlin 13
Tel. (030) 3 82 80 34
Telex 185 544 wgbln d
Fax (030) 3 82 87 43

Wandel & Goltermann
Technisches Büro Düsseldorf
Am Rathaus 1
4020 Mettmann
Tel. (02104) 78 21
Fax (02104) 78 24

Wandel & Goltermann
Technisches Büro Frankfurt
Schwalbacher Straße 52
6236 Eschborn
Tel. (06196) 48 26 98
Fax (06196) 48 11 22

Wandel & Goltermann
Technisches Büro Hamburg
Moltkestraße 50 b
2000 Hamburg 20
Tel. (040) 4 20 28 28, 29
Fax (040) 4 20 57 55

Wandel & Goltermann
Technisches Büro München
Josef-Retzer-Straße 57
8000 München 60
Tel. (089) 83 70 37
Fax (089) 88 77 10

Wandel & Goltermann
Technisches Büro Süd
Arbachtalstraße 6
Postfach 1262
7412 Eningen u.A.
Tel. (07121) 86 15 10
Telex 7 29 833 wug d
Fax (07121) 86 20 28

Wandel & Goltermann
Technisches Büro DBP Telekom
Arbachtalstraße 6
Postfach 1262
7412 Eningen u.A.
Tel. (07121) 86 15 18
Telex 7 29 833 wug d
Fax (07121) 86 21 45

Schweiz

Wandel & Goltermann (Schweiz) AG
Postfach 779
Morgenstrasse 83
CH-3018 Bern 18
Tel. 031-55 65 44
Tlx. 9 12 350 wg ch
Fax 031-55 47 07

Österreich

Wandel & Goltermann Ges.m.b.H.
Postfach 13
Elisabethstraße 36
A-2500 Baden
Tel. (02252) 85 52 10
Telex 14 375 wgo a
Fax (02252) 85 52 12 30

Weltweit

Internationaler Informations-Service
Wandel & Goltermann VMW
Postfach 1262
D-7412 Eningen u.A.
Fed. Rep. of Germany
Tel. + 49 7121 860
Fax + 49 7121 8 84 04
Telex 7 29 833 wug d

Wandel & Goltermann unterhält ein weltweites Vertriebs- und Servicenetz mit 19 Vertriebsgesellschaften und über 60 Vertretungen in allen fünf Kontinenten. Wir versorgen Sie gern mit weiterer Information und helfen Ihnen bei der Lösung Ihrer individuellen Meßaufgaben. Wenden Sie sich bitte an die nächstgelegene Vertriebsstelle oder an unseren internationalen Informations-Service.

Wandel & Goltermann Worldwide Sales Organization

Europe

Austria
Wandel & Goltermann Ges.m.b.H.
P.O. Box 13
Elisabethstraße 36
A-2500 Baden
Tel. 022 52-8 55 21-0
Telex 14 375 wgo a
Fax 022 52-85 52 12 30

Belgium/Luxembourg
Wandel & Goltermann nv/sa
Imperialstraat 10
B-1930 Zaventem
Belgium
Tel. 2-725 18 19
Fax 2-725 41 42

The Netherlands
Wandel & Goltermann bv
Monnickskamp 8
NL-1273 JS Huizen
Tel. 02152-66 122
Fax 02152-6 79 37

France
Wandel & Goltermann France
46 bis, rue Pierre Curie
B. P. 10
Zone Industrielle Les Gâtines
F-78372 Plaisir Cédex
Tél. (1) 30 81 50 50
Telex 698 955 f
Fax (1) 30 55 87 75

Germany
Wandel & Goltermann
Vertriebsgesellschaft
P.O. Box 1262
7412 Eningen u.A.
F.R. of Germany
Tel. 07121-86 15 11
Telex 7 29 833 wug d
Fax 07121-86 20 28

Italy
A.E.S.S.E. S.P.A.
Viale Umbria 32-36
I-20 135 Milano
Tel. 2-546 4741/2/3, 55 181 162
Telex 31 22 93 AESSE i
Fax 2-545 0701

United Kingdom
Wandel & Goltermann Sales Ltd.
Progress House
412 Greenford Road
Greenford, Middlesex, UB6 9AH
Tel. 081-5 75 30 20
Telex 934 489 waguk g
Fax 081-5 75 56 29

Spain
Wandel & Goltermann S.A.
Sucursal de España
Bueso Pineda No 7
Apartado de Correos 48008
E-28080 Madrid
Tel. 15 19 4624/15 19 48 24
Fax 15 19 59 81

Sweden
Wandel & Goltermann AB
Box 6044
Ellen Keys Gata 60
S-126 06 Hägersten
Tel. 8-88 04 80
Fax 8-88 38 90

Switzerland
Wandel & Goltermann (Schweiz) AG
P.O. Box 779
Morgenstrasse 83
CH-3018 Bern 18
Tel. 031-55 65 44
Telex 912 350 wg ch
Fax 031-55 47 07

Turkey
Wandel & Goltermann
Irtibat Bürosu
Farabi Sokak no. 17/1
Kavaklidere - Ankara
Tel. 4-167 64 90/167 64 91
Fax 4-167 64 92

North America

Canada
Wandel & Goltermann Inc.
21 Rolark Drive
Scarborough, Ontario M1R 3B1
Tel. 416-291-7121
Fax 416-291-26 38

USA
Wandel & Goltermann Inc.
2200 Gateway Centre Blvd.
Morrisville, NC 27560-9228
Tel. 919-460-33 00
Fax 919-481-43 72

Latin America

Argentina
Wandel & Goltermann S.A.
Montaneses 2599
1428 Buenos Aires
Tel. 1-784 66 42
Telex 24 543 wglas ar
Fax 111 27 88

Brazil
Wandel & Goltermann
Instrumtacào Ltda. & Cia.
Av. Engo L. C. Berrini, 936-Cj. 91
Herr M. Steube
04571 Sào Paulo - SP
Tel. 11-241 15 88
Telex 11 56 569 wgep br
Fax 11-241 96 62

Guatemala
Wandel & Goltermann & Co
Gerencia Regional Norte
Apartado Postal 2761
01901 Guatemala Ciudad
Tel. (2) 31 80 65
Telex 5 432 wagola gu
Fax (2) 31 86 82

Mexico
Wandel & Goltermann de México,
S.A. de C. V.
Rio Rhin No. 22 Penthouse 1
Col. Cuauhtémoc
06500 México D.F.
Apartado Postal 57090
06501 México, D.F.
Tel. 703-2430, 703-2900
Fax 703-23 49

Asia

Middle East and India
Wandel & Goltermann
Export Division
P.O. Box 1262
7412 Eningen u.A.
F.R. of Germany
Tel. 07121-86 16 83
Telex 7 29 833 wug d
Fax 07121-86 21 55

East- and South East Asia:

Regional Headquarter
Wandel & Goltermann Ltd.
1905 Bond Centre, West Tower
89 Queensway, Central Hong Kong
Tel. (+852) 868-3113
Telex 77 787 wango hx
Fax (+852) 868-5482

Singapore
Wandel & Goltermann
Representative Office for
South East Asia
14-11 Manhattan House
151 Chin Swee Road
Singapore 0316
Republic of Singapore
Tel. +65 733-07 22
Telex 38 133 WANDEL rs
Fax +65 732-89 09

Republic of Korea
Wandel & Goltermann Ltd.
5th Floor, Hayan Building
153-55 Samsung 1-dong
Kangnam-ku
Seoul 135-091
Republic of Korea
Tel. +82(2)563-22 36/7
Fax +82(2)563-22 39

Japan
Wandel & Goltermann K.K.
German Industry Center 207
1-18-2 Hakusan, Midori-ku
Yokohama, Japan 226
Tel. 45-931-57 25
Fax 45-931-57 28

Africa

Wandel & Goltermann
Export Division
P.O. Box 1262
7412 Eningen u.A.
F.R. of Germany
Tel. 07121-86 16 83
Telex 7 29 833 wug d
Fax 07121-86 21 55

Australia/Papua New Guinea and Pacific Islands

Australia
Wandel & Goltermann Pty. Ltd
P.O. Box 419
World Trade Centre
Melbourne, Victoria 3005
Tel. 03-690 67 00
Telex AA 34 801 wg aus
Fax 03-690 67 50

For other areas not listed contact:

International Information Service
Wandel & Goltermann
VMW
P.O. Box 1262
D-7412 Eningen u.A.
F.R. of Germany
Tel. +49 7121 860
Telex 7 29 833 wug d
Fax +49 7121 8 84 04

A closely linked network of 19 affiliated companies and more than 60 agencies around the world ensures that our customers receive the be possible advice in solving specific measurement problems. For more detailed information, please turn to your local sales agency or to our International Information Service.

Sociétés de vente Wandel & Goltermann

France
Wandel & Goltermann France
46 bis, rue Pierre Curie
B.P. 10
Zone Industrielle Les Gâtines
F-78372 Plaisir Cédex
Tél. (1) 30 81 50 50
Tlx. 698 955 f
Fax (1) 30 55 87 75
Télétex 933-130 559 429 = wandelfr

Canada
Wandel & Goltermann Inc.
21 Rolark Drive
Scarborough, Ontario M1R 3B1
Tel. 416-291-7121
Fax 416-291-2638

Belgique/Luxembourg
Wandel & Goltermann nv/sa
Imperialstraat 10
B-1930 Zaventem
Tel. 2-7 28 18 19
Fax 2-7 25 41 42

Afrique
Wandel & Goltermann GmbH & Co.
Export Division
P.O. Box 1262
D-7412 Eningen u.A.
F.R. of Germany
Tel. +49 7121 86 16 83
Telex 7 29 833 wug d
Fax +49 7121 86 21 55

Suisse
Wandel & Goltermann (Schweiz) AG
Postfach 779
Morgenstrasse 83
CH-3018 Bern 18
Tel. 031-55 65 44
Tlx. 9 12 350 wg ch
Fax 031-55 47 07

Autres pays contactez:
Service d'information international
Wandel & Goltermann
VMW
P.O. Box 1262
D-7412 Eningen u.A.
F.R. of Germany
Tel. +49 7121 8 60
Telex 7 29 833 wug d
Fax +49 7121 8 84 04

Wandel & Goltermann possède un réseau mondial de distribution et de maintenance, avec 19 filiales et plus de 60 représentations sur les cinq continents. Nous vous fournissons les informations et l'aide nécessaires pour trouver une solution adaptée à vos besoins de mesure spécifiques. Adressez-vous à la filiale la plus proche ou à notre service d'informations international.

www.manualsplus.com
1028174

Wandel & Goltermann
Elektronische Meßtechnik